Ian O'Connor

British national

Lyon Institute of Nanotechnology (INL)
Ecole Centrale de Lyon – University of Lyon
36, avenue Guy de Collongue
F-69134 Ecully cedex, France
Tel: +33 645 478 120
Email: ian.oconnor@ec-lyon.fr
Website: ioconnor930.github.io
LinkedIn: fr.linkedin.com/in/ian-o-connor-7592153
ORCID: 0000-0002-6238-9600
Google Scholar: SDTr6iEAAAAJ



Biography

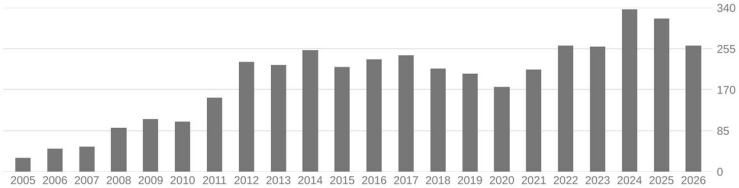
Ian O'Connor (IEEE S'95-M'98-SM'07) is Distinguished Professor of Cross-Layer Design for Energy-Efficient Computing in the Department of Electronic, Electrical and Control Engineering at Ecole Centrale de Lyon, France. He is joint head of the Electronics group at the Lyon Institute of Nanotechnology, Director of the SoC^2 research network, and co-director of the France 2030 PHOENIX program. From 2008 to 2022, he also held a position of Adjunct Professor at Ecole Polytechnique de Montréal, Canada. His research interests include novel computing and interconnect architectures based on emerging technologies, associated with methods for design exploration. He has authored or co-authored well over 300 peer-reviewed book chapters, journal publications, conference papers and patents, has held various positions of responsibility in the organization of several international conferences and has been workpackage leader or scientific coordinator for several national and European projects. He also serves as an expert with Collège Numérique France 2030, International Roadmap for Devices and Systems (IRDS) Systems and Architectures International Focus Team, International Federation for Information Processing (IFIP) WG10.5 (Design and Engineering of Electronic Systems), is Vice-President for Publications in the IEEE Council for Electronic Design Automation (CEDA), is Chair of the Main Board of the European Design Automation Association (EDAA), Area Editor (Circuits and Emerging Technologies) for IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems and Associate Editor for IEEE Trans. Circuits and Systems for Artificial Intelligence.

Highlights

- **Publications:** 300+ peer-reviewed works: 66 journal articles, 4 books, 22 book chapters, 235 conference papers (52 invited/keynote), 7 patents; 4,326 citations, h-index 30 (Google Scholar, November 2026)
- **Supervision:** 40 PhD theses (31 defended) and 12 postdoctoral researchers; graduates now at IBM Research, CERN, EPFL, University of Utah, NTU Singapore, CEA-LETI, STMicroelectronics, Cadence, Synopsys and Siemens EDA, and in start-ups (eVaderis, Luceda)
- **Research leadership:** scientific coordinator of 9 regional, national and international projects (about 4 M€ in total budget) and work-package leader in 19; about 7.3 M€ in partner funding secured for INL/ECL across 30 funded projects since 2001; scientific co-director of the France 2030 PHOENIX program (17 M€) and co-coordinator of the CAMELIA targeted project LEAF
- **Community leadership:** IEEE CEDA Vice-President for Publications; Chair of the EDAA Main Board; Director of the CNRS GdR SoC2; Area Editor, IEEE TCAD; Associate Editor, IEEE TCASAI; General Chair of DATE 2023 and Program Chair of DATE 2021
- **Recognition:** IEEE CEDA Outstanding Service Recognition (2024), IEEE TTTC Outstanding Service Award (2023), Best Paper Awards at IFIP/IEEE VLSI-SoC (2025) and IEEE NEWCAS (2011), National Scientific Excellence Award (2001–2028)

Citation indices (source: Google Scholar)

15/11/2026	*All*	*Since 2021*
Citations	4326	1651
h-index	30	20
i10-index	105	38



Professional experience

Distinguished Professor, Electronic Electrical and Control Engineering Department	2007–present
Ecole Centrale de Lyon, Ecully (FR)	
Also Joint Head of Electronics Group	2007–present
Also Vice-Director	2006–2010
Lyon Institute of Nanotechnology JRU 5270	
Also Director, GdR SoC^2 (System-on-Chip, Embedded Systems and IoT) network	2018–present
CNRS (FR)	
Also Adjunct Professor, Computer and Software Engineering Department	2008–2022
Ecole Polytechnique de Montréal (CA)	
Associate Professor, Electronic Electrical and Control Engineering Department	1998–2007
Ecole Centrale de Lyon, Ecully (FR)	
Senior CAD Engineer, Design Technology Centre	1997–1998
Philips (now NXP) Semiconductors, Southampton (UK)	
Research and teaching assistant, Microelectronics Department	1993–1997
Institut Supérieur d'Electronique du Nord (ISEN), Lille (FR)	
Network engineer	1993
CIMM-SDI, Villeneuve d'Ascq (FR)	

Education

Professorial Dissertation (Habilitation à Diriger des Recherches) in Electronics	Oct. 2005
"Physically heterogeneous systems on chip: design methodologies and optical interconnect systems"	
Ecole Centrale de Lyon, Ecully (FR)	
PhD (with distinction) in Electronics *"Automated design of current memory cells"*	Nov. 1997
Director: J.N. Decarpigny; Advisor: A. Kaiser	
University of Lille I (FR)	
MSc Electrical Engineering (European Program)	Jul. 1992
University of Essex, Colchester (UK) / ESIEE, Paris (FR) / University of Karlsruhe (DE)	
BEng 2/i Electronic Systems Engineering	Jul. 1990
University of Essex, Colchester (UK)	

Principal scientific responsibilities

- **Joint Head of Electronics group** (25 Profs. and Assoc. Profs.) at Lyon Institute of Nanotechnology
- **Co-Director of the PHOENIX program** (France 2030-funded 17M€ research initiative involving CEA-LIST and 15 CNRS JRUs to establish a national hub for advanced integrated circuit design using chiplets, AI-augmented EDA methods, hardware-software co-design)
- **Advisor for 12 postdoctoral fellowships, 40 PhDs (1 recipient of Best Centrale Innovation Thesis Award), 28 MSc internships**. PhD graduates now at Beijing University (CN), CERN (FR), EPFL (CH), University of Utah (USA), Nanyang Technological University (SG), GCI Science & Technology (CN), IBM Research (USA), ID Quantique (CH), CEA-LETI (FR), Corning Optical Communications (PL), Dolphin Integration (FR), Groupe SEB (FR), Siemens EDA (FR), Schlumberger (FR), STMicroelectronics (FR), Cadence (USA), Synopsys (USA), UFRGS/INOVA-ME (BR), startups: Changsha Funeng Biotechnology (CN), eVaderis (FR), Luceda (BE), Tiino Techmation (IN)
- **Workpackage leader for 3 regional projects, 9 national projects, 7 European projects**
- **Scientific coordinator for 3 regional projects, 5 national projects, 1 international project**
- **General Chair of 4 international conferences, Program chair of 5 international conferences**, Topic chair of 7 international conferences (multiple editions), Finance chair of 1 international conference, Executive Committee member and Special Day chair of 1 international conference, regular Technical Program Committee member of 9 international conferences, Co-founder and Program Chair of 1 Winter School
- Member of French SoC^2 Research Network steering committee: Heterogeneous Systems co-chair (2007–2012), vice-director since 2012, **director since 2018**
- **Expert with HCERES (French High Council for Evaluation of Research and Higher Education)** – evaluation committee member for LIEN (2008), GREEN (2008), IJL (2016), EpOC (2017), IEMN (2019), ESYCOM (2019)

research laboratories, evaluation committee chairman for IEMN (2024) laboratory, evaluation committee member for 1 Masters program (2010)

- **Visiting Professor** at Ecole Polytechnique de Montréal, Canada in December 2005, January 2008. **Adjunct Professor** at same institution 2008–2022
- **IEEE Senior Member since 2007, Vice-President IEEE Council for Electronic Design Automation (CEDA) (VP Initiatives 2020–2023, VP Technical Activities 2024–2025, VP Publications 2026–2027)**, member of IET, ACM/SIGDA, Club EEA
- Regular reviewer for several journals (IEEE, Elsevier, Springer)
- Reviewer of several national (ANR), industrial (BPI) and international (ISF, SNSF) projects
- **Member of ANR Scientific Evaluation Committee on Micronanoelectronics for data processing** (2014, 2015 (**vice-president**), 2018), **ANR DeepGreen Deployment of embedded AI solutions on specific hardware targets** (2022). **Proposal Evaluator** for **H2020-FETOPEN, H2020-ERC, Horizon Europe-EIC Pathfinder 2021–2025, Horizon Europe-EIC Accelerator 2025–2026, Horizon Europe-EIC Widera 2025, Horizon Europe-Digital Emerging 2021–2023, Horizon Europe-REA MSCA Engineering 2022–2025, ESF** (2018–2023), Technical Due Diligence for **European Innovation Council and SMEs Executive Agency (2026)**. Member of intermediate and final ANR project review boards (2015, 2016)
- **Member of review boards for 4 EU-funded projects** (H2020-ICT TOP-HIT, CONNECT, TERIPHIC, H2020-FET SPICE) – annual progress reviews (2015–2023); and for 1 Ifremer-funded project (POPSTAR, 2016–2018)
- **Expert with the French Observatory of Micro-Nanotechnologies (OMNT)** 2005–2017 (Nanodevices, Nanoelectronics groups, New computing paradigms and Neuromorphic Computing focus groups)
- **Expert with Collège Numérique France 2030** since 2023
- Nanotechnology Workshop Chairman for Disruptive Technologies Day (French CNRS-INSIS / French Aerospace Industry Group), 2016
- **Member of IFIP (International Federation for Information Processing) WG10.5 (Design and Engineering of Electronic Systems)** since 2009
- **Member of International Roadmap for Devices and Systems (IRDS) IFT Systems and Architectures** since 2022
- Member of the Main Board of the **European Design Automation Association (EDAA)** since 2021, Vice-Chair 2024–2025, **Chair since 2026**, Chair of EDAA Outstanding Dissertation Award (2024–2026)
- Member, Alliance for digital science and technology – Hardware technologies and devices WG, 2010–2017
- Member, Multidisciplinary Institute in Artificial Intelligence (MIAI) Grenoble Alpes – Scientific Board, 2021-
- Member, Steering committee French Priority Research and Equipment Program on Artificial Intelligence (2022)
- Member of steering committee for "Devices, Systems, Computing and Software" track in Rhône-Alpes Region ARC (Academic Research Community) "Information and Communication Technology " 2012–2017
- **Elected member of French National Universities Council**, section 63 Electrical and Electronic Engineering, Photonics and Systems (2015–2019)
- **External reviewer for 90 PhD theses (10 international) and chairman for 37 PhD thesis defenses**, **external reviewer for 18 professorial dissertations and chairman for 3 professorial dissertation defenses**
- **Associate Editor** for **IEEE Trans. Multi-Scale Computing Systems** (2015–2018), **IET Computers and Digital Techniques** (2019–2022), **IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems** (2022–2023, 2024–2025), **IEEE Trans. Circuits and Systems for Artificial Intelligence** (2024–present, second term from 2026); **Area Editor (Circuits and Emerging Technologies) IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems** (2026–2027)
- External member of faculty recruitment boards for 5 Full Professor positions, 5 Associate Professor positions
- Recipient of **National Scientific Excellence / Research Award** (6 consecutive 4-year awards and 1 3-year award), 2001–2028
- Recipient of **IEEE TTTC (Test Technology Technical Council) Outstanding Service Award** 2023
- Recipient of **IEEE CEDA (Council for Electronic Design Automation) Outstanding Service Recognition Award** 2024

Publications summary

- 66 articles published in refereed publications (journals)
- 22 book chapters, 4 books (3 edited), 7 patents

- 52 invited/keynote and 183 regular articles (2 recipients of Best Paper Award) published in refereed international conference proceedings
- 83 workshops, seminars, tutorials and panel discussions, 7 scientific outreach publications
- H-index 30 – i10-index 105 – 4326 citations

Teaching activities at Ecole Centrale de Lyon, University of Lyon

B3	Electronic Systems (M) – ECL Engineering diploma	L, C, S
M1	*[past] Adaptive filters – ECL Engineering diploma*	*L*
M1	*[past] Advanced system electronics (M) – ECL Engineering diploma*	*L, C, S*
M1	Digital architectures for computing and data processing (M) – ECL Engineering diploma	L, C, S
M1	Introduction to System Design – MSc Nanoscale Engineering	L
M2	*[past] Analog and mixed-signal integrated circuit design (M) – ECL Engineering diploma*	*L, C, S*
M2	Design choice management in Electrical Engineering (M) – ECL Engineering diploma	L
M2	*[past] DSP and telecom systems (M) – ECL Engineering diploma*	*L, S*
M2	Heterogeneous microelectronic design (M) – MSc EEEA / Embedded Systems Electronics	L
M2	*[past] Green computing (M) – ECL Engineering diploma*	*L, C*
M2	*[past] Autonomous microsystems (M) – ECL Engineering diploma*	*L, C, S*
M2	Sustainable and Trustworthy Hardware Architectures for AI (M) – ECL Engineering diploma	L, C
M2	Analog Computing for Artificial Intelligence (M) – ECL Engineering diploma	L, C, S
M2	Methods for integrated system design – MSc EEEA / Embedded Systems Electronics	L
M2	*[past] Micronanoelectronic circuit design (M) – ECL Engineering diploma*	*L, C, S*
M2	*[past] Memories for Internet of Things – ECL Engineering diploma*	*L, S*
M2	Microsystems, microsensors, microfluidics (M) – ECL Engineering diploma	L, C
M2	*[past] Multiphysics Systems Integration (M) – MSc Nanoscale Engineering*	*L*
M2	Nanoelectronics and information technology – MSc Nanoscale Engineering	L, S
M2	System Design Engineering – MSc Industrial Engineering	L
M2	*[past] System on chip design methodology – ECL Engineering diploma*	*L*
M2	*[past] VLSI system architectures – ECL Engineering diploma*	*S*

Bn=nth year of Bachelor level Mn=nth year of Master level; M=course manager; L=lectures; C=problem classes; S=laboratory sessions

Administrative responsibilities

Elected member of ECL Scientific Council	2021–2025
Vice-Chairman of ECL examination board for 2023 graduation track	2021–2023
Member of MSc EEEA management board (ECL chair until 2022, joint head of ESE track)	2012–present
Elected member of ECL EECE Department Council	2011–present
Head of Electronics Lecturing Group at ECL	2011–2019
Member of ECL examination board for 2017 graduation track	2015–2017
Chairman of ECL examination board for 2010 graduation track	2007–2009
Vice-Director of Lyon Institute of Nanotechnology (ECL site manager)	2006–2010
Elected member of ECL Electrical and Information Sciences Board	2001–2007
Elected member of ECL Scientific Council	2001–2005
Member of ECL International Relations Board	1999–2011

Current research activities at Lyon Institute of Nanotechnology (INL)

The pursuit of Moore's Law is slowing and the exploration of alternative devices is underway to replace the CMOS transistor and traditional architectures at the heart of data processing. My research, as joint head of the Electronics group at the Lyon Institute of Nanotechnology, focuses on the development of novel energy-efficient computing architectures based on advanced, emerging and alternative devices, specifically exploring the contributions of:

- devices for advanced and emerging logic and computation (vertical nanowire FETs, ferroelectric non-volatile devices), requiring new logic gate structures and rethinking of computing paradigms and associated architectures;
- devices for in-network computing and data transport in emerging manycore architectures (optical interconnects based on silicon photonics), requiring novel communication topologies exploiting wavelength vectors, and methods for performance comparison against conventional interconnect structures;
- "More than Moore" systems using new integration technologies (vertical integration in three dimensions, heterogeneous integration), requiring new design methods and tools to manage both complexity and heterogeneity.

Energy efficient edge computing based on advanced and emerging devices and paradigms

Data size and functionality requirements for computing are increasing, according to the expectation that hardware performance will continue to improve, irrespective of the actual implementation. This is particularly true for emerging distributed computing paradigms for the Internet of Things, such as Edge Computing and Fog Computing, which are placing extraordinarily stringent constraints on computing hardware performance. Such paradigms are necessary to guarantee low-latency, secure and contextualized computation on inhomogeneous sensory data, as close as possible to the data source. This usually implies that energy sources are limited and consequently, that Edge Computing hardware energy efficiency must be maximized. At the system level, it is widely accepted that reconfigurable logic hardware can significantly reduce energy per computation, particularly as the problem size increases. Such hardware can be placed in the data acquisition chain between the raw sensor output and the central computing core and given the task of pre-processing the data in order to reduce the core workload. It can also be placed in the data processing chain between the memory banks and the central computing core to accelerate specific computation tasks, reducing latency and energy costs. Therefore, the use of energy-efficient, reconfigurable hardware accelerators is mandatory to unlock the full potential of Edge Computing.

In this context, the emergence of new research devices offers the opportunity to provide novel building blocks, to elaborate non-conventional techniques for logic design and consequently to reconsider the paradigms of computing architectures (such as approximate computing, stochastic computing, and neuromorphic computing) to achieve orders of magnitude improvements in the conventional figure of merit (MIPS / volume*power). Highlights of previous work, based on specifically exploiting the additional functionality of 4-terminal devices for reconfigurability purposes include:

- design and patenting of ultra-fine grain reconfigurable architectures and cells based on ambipolar double-gate CNTFETs and on double-gate MOSFETs
- development and patenting of interconnect topologies and architectures based on reconfigurable cells
- development of logic synthesis techniques for ambipolar reconfigurable logic and mapping and synthesis flows for matrix-based architectures

Currently funded work is focusing on:

- building new 3D logic circuits and computing architectures based on vertical nanowire FETs. Such devices favor regular logic structures with multiple switches in series based on techniques such as majority gate logic or pass-gate logic. This work therefore aims to prove enhanced logic functionality and logic circuit operation in terms of propagation delay, dynamic and static power consumption, resilience to temperature and supply voltage variation, and to assess the technology roadmap improvements and the associated logic performance metrics.
- exploring low-power logic cell architectures based on ferroelectric capacitors and FETs (FeFETs). HfO_2-based ferroelectric non-volatile devices are CMOS-compatible, fast, low power and high endurance, and could greatly enhance energy-efficiency and allow flexibility for finer grain logic and memory. This will give unprecedented flexibility for fine-grain logic-in-memory (LiM) circuits, which allows data storage close to logic circuits, reduces energy cost of data transfer, allows smart gating for "normally-off" computing and opens the way to real demonstration of novel energy-efficient computing paradigms.

This work is the result of 10 PhD theses (3 ongoing) and 4 postdocs, supported by several projects at the national level (ACI Nanosys, ANR^{ARPEGE} Nanograin, ANR^{PNANO} Multigrilles, LST Grilles-CMOS, ANR^{AAPG} LEGO, PEPR Electronique AC3 FerroFutures) and at the European level (H2020-ICT 3εFerro, H2020-FETPROACT FVLLMONTI, Horizon Europe Ferro4EdgeAI).

Collaborations: CEA-LETI/LIST/IRAMIS (FR), IMS (FR), IM2NP (FR), LIRMM (FR), IEF (FR), IEMN (FR), UMP CNRS-Thales (FR), LAAS (FR), NaMLab (DE), EPFL (CH), Global TCAD Solutions (AT), Ecole Polytechnique de Montréal (CA), University Notre Dame (US).

Silicon photonics for high-performance and in-network computing

The emergence of very high-performance processors is necessary to achieve future required application performance in terms of resolution (audio, video and computing) and CPU power / total MIPS (real-time encoding-decoding, data encryption-decryption, artificial intelligence). Distributed manycore architectures are key to achieve such performance levels but require organized high-speed communication between processors, capable of supporting an aggregate data rate exceeding 100TB/s. Metallic interconnect is highly inefficient in this role due to unachievable tradeoffs between design parameters. Silicon photonics, and the concept of on-chip optical data transport, is a potential technological solution to alleviate some of these issues involved in exchanging data between cores in SoC architectures, and in particular that of energy (around 1pJ/bit/mm in metallic interconnect). This research track aims to contribute to the ongoing assessment of the suitability of integrated optical interconnect for on-chip data transport. In this context, we have contributed to the state of the art at world-class level:

- Predictive performance assessment of optical interconnect per technology node. We were the first to quantify in detail the performance levels for future technology nodes.
- Development of several passive and active optical network on chip topologies exploiting wavelength and targeting real communication requirements.
- Modeling and simulation at the system level of optical networks on chip integrated with an industrial communication protocol.

Currently funded work is focusing on the design of energy-efficient broadcast-aware nanophotonic interconnect that goes below the 0.1pJ/bit energy consumption barrier for an aggregated 100TB/s total bandwidth and on the association of stochastic computing with PCM-enhanced silicon photonics to implement a matrix multiplication accelerator for in-network neural networks.

This work is the result of 14 PhD theses (1 ongoing) and 5 postdocs, conducted in the framework of several national (RMNT Heteropt, LabEx CominLabs 3D-Optical-Manycores, ANR^{AAPG} OpticALL^2, ANR^{AAPG} Octane, PEPR-IA Adapting, PEPR-CAMELIA LEAF, PEPR-CAMELIA CHALICE), European (FP6-IST PICMOS, FP7-ICT WADIMOS, FP7-ICT HELIOS, Horizon Europe Neuropuls) and international (Horizon 2020 MSCA REDI) projects.

Collaborations: CEA-LETI (FR), INRIA-IRISA (FR), C2N (FR), Mentor Graphics (FR), Kalray (FR), ICB (FR), IMEC (BE), STMicroelectronics (IT), Ecole Polytechnique de Montréal (CA), Concordia University (CA), Hong Kong University of Science and Technology (CN), RMIT (AUS).

Design Technology Co-Optimization methods for heterogeneous integrated systems

Heterogeneous integrated systems are based on devices that do not necessarily scale according to "Moore's Law" and provide functional diversification i.e. additional value in different ways, such as power generation and management, or sensing and actuating with motion sensors (accelerometers, gyroscopes and magnetometers), environment sensors (light level, color, temperature, pressure, humidity), or biosensors (eNoses, blood pressure, pH). The "More-than-Moore" (MtM) approach allows for such non-digital functionalities to migrate from the system board-level into the package (SiP) or onto the chip (SoC). The number of heterogeneous functions is growing at a rate of 1.3x per year in consumer portable applications such as smartphones, and opportunities are growing for heterogeneous component integration with the advent of technologies such as 2.5D and monolithic 3D. It is anticipated that the market of analog and heterogeneous ICs will experience an explosion in the 2020s, due to the strong demand of billions of connected objects with intelligent sensors, in the context of Big Data and IoT. Future integrated "sensor hubs" will require the simultaneous analysis and fusion of data from a wide range of sensor types for full interpretation of device state and situation.

However, while MtM process and device technology have progressed, the development of enabling design technologies has not kept pace. Some of the many design technology challenges are: heterogeneous system partitioning and simulation; analog and mixed-signal design technologies for sensors and actuators; new methods

and tools for co-design and co-simulation of SIP, MEMS, and biotechnology. Without radically new design technology, it will be impossible to realize the full potential of MtM technology.

This research track contributes to the efficient design of MtM ICs by providing innovative design techniques and tools for the multi-physics parts of these systems. The complexity of this task, with many inter-related degrees of freedom and performance metrics, is similar to searching for the center of a very large three-dimensional maze with a flashlight and no map. The work targets the solving of fundamental issues with the way in which heterogeneous components are designed and integrated into systems during the design process. The objective is to examine ways in which to predictively extract and exploit system and circuit design information, and apply it in the context of a multi-physics sensor hub application.

Highlights of recent and current work include:

- the implementation of a meta-optimization strategy for early, deterministic and optimal floorplanning of 3D ICs taking into account planar and vertical interconnect resources, inter-core network traffic, thermal variations and manufacturing cost;
- the development and patenting of a predictive method for the synthesis of multi-physics systems based on a hierarchical approximation and combination of sub-system Pareto fronts. Tools associated with this method are the focus of a laboratory spinoff project;
- the proposal of a new method to estimate the bounds of performance variability in analog circuits, combining design of experiments techniques (to extract and model performance variability) with the Cornish-Fisher expansion (to approximate the quantile distribution);
- the efficient extraction of predictive models based on Pareto-fronts and a fast graph-based approach, and their extension to n-performance design spaces using the Hyper-Space Diagonal Counting (HSDC) methodology

This work is the result of 16 PhD theses (2 ongoing) and 3 postdocs, and has been carried out in the framework of several projects under my scientific coordination (regional program Osmose, Auto-BAW, Centre Jacques Cartier projects, CNRS PICS, Nano2008 / Nano2012 agreements, ANR-PNANO 3D-IDEAS, ANR-AAPG HELICITY, PEPR Electronique CHOOSE, PEPR-PHOENIX) as well as Eureka projects CATRENE 3DIM3 and CATRENE H-Inception).

Collaborations: CEA-LETI/LIST (FR), STMicroelectronics (FR), iCube (FR), IMEP-LAHC (FR), LCIS (FR), Asygn (FR), Intento Design (FR), TIMA (FR), TU Delft (NL), Fraunhofer (DE), Ecole Polytechnique de Montréal (CA), University Notre Dame (US).

List of publications for Ian O'Connor

Underlined author names in the lists below indicate PhD students and postdoctoral researchers supervised by I. O'Connor.

Selected publications

- I. O'Connor, J. Liu, F. Gaffiot, F. Prégaldiny, C. Lallement, C. Maneux et al., "CNTFET Modeling and Reconfigurable Logic Circuit Design," IEEE Trans. Circuits and Systems I, 54(11), 2007.
  Introduced ultra-fine-grain reconfigurable logic built on ambipolar double-gate carbon-nanotube FETs.
- I. O'Connor, F. Tissafi-Drissi, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, J. Van Campenhout, D. Van Thourhout, "Systematic Simulation-Based Predictive Synthesis of Integrated Optical Interconnect," IEEE Trans. VLSI Systems, 15(8), 2007.
  Predictive, technology-node-aware synthesis and assessment of on-chip optical interconnect.
- H. Filiol, I. O'Connor, D. Morche, "Analog IC variability bound estimation using the Cornish-Fisher expansion," IEEE Trans. CAD, 31(9), 2012.
  Statistical bounds on analog performance variability from a small number of simulations.
- F. Frantz, L. Labrak, I. O'Connor, "3D IC floorplanning: automating optimization settings and exploring new thermal-aware management techniques," Microelectronics Journal, 43(6), 2012.
  Meta-optimization for thermal- and interconnect-aware early floorplanning of 3D ICs.
- H. Li, A. Fourmigue, S. Le Beux, I. O'Connor, G. Nicolescu, "Towards maximum energy efficiency in nanophotonic interconnects with thermal-aware on-chip laser tuning," IEEE Trans. Emerging Topics in Computing, 6(3), 2018.
  Run-time thermal-aware laser control for energy-efficient optical networks-on-chip.
- A. Perodou, A. Korniienko, G. Scorletti, M. Zarudniev, J.B. David, I. O'Connor, "Frequency Design of Lossless Passive Electronic Filters: a state-space formulation of the direct synthesis approach," IEEE Trans. Circuits and Systems I, 68(1), 2021.
  A control-theory formulation for the direct synthesis of passive filters.
- C. Marchand, I. O'Connor, M. Cantan, S. Slesazeck, T. Mikolajick, "A FeFET-based hybrid memory accessible by content and by address," IEEE J. Exploratory Solid-State Computational Devices and Circuits, 8(1), 2022.
  Ferroelectric logic-in-memory combining content- and address-based access in one array.
- M. Abdalla, C. Zrounba, R. Cardoso, P. Jimenez, G. Ren, A. Boes, A. Mitchell, A. Bosio, I. O'Connor, F. Pavanello, "Minimum complexity integrated photonic architecture for delay-based reservoir computing," Optics Express, 31(7), 2023.
  A minimal integrated photonic reservoir computer for neuromorphic processing.
- R. Cardoso, C. Zrounba, M. Abdalla, M. Gomes de Queiroz, P. Jimenez, I. O'Connor, S. Le Beux, "Reconfigurable Photonic GEMM Based on Phase-Change-Materials and Stochastic Computing," IEEE/Optica J. Lightwave Technology, 2024.
  Photonic matrix multiplication combining phase-change materials with stochastic computing.
- M. Soliman, C. Marchand, A. Mahmoudi et al., I. O'Connor, A. Ouerghi, J.F. Dayen, "Van der Waals Inverted-Floating-Gate Transistors for Artificial Intelligence Electronics," ACS Nano, 19(19), 2025.
  2D-material memory transistors for AI hardware.

Books

1. *Design Technology for Heterogeneous Embedded Systems*, ed. G. Nicolescu, I. O'Connor, C. Piguet, Springer, 477 p., 266 illus., ISBN 978-94-007-1124-2 (2012)
2. P.E. Gaillardon, I. O'Connor, F. Clermidy, *Disruptive Logic Architectures and Technologies: From Device to System Level*, Springer, 187p., ISBN 978-14-614-3057-5 (2012)
3. *Integrated Optical Interconnect Architectures and Applications in Embedded Systems*, ed. I. O'Connor, G. Nicolescu, Springer, 281p., ISBN: 978-14-419-6192-1 (2013)
4. *System-on-Chip in the nanoscale era: design, verification and reliability*, ed. T. Hollstein, J. Raik, A. Tšertov, S. Kostin, I. O'Connor, R. Reis, Springer, 232p., ISBN: 978-3-319-67103-1 (2017)

Book chapters

1. F. Mieyeville, M. Brière, I. O'Connor, F. Gaffiot, G. Jacquemod, "A VHDL-AMS library of hierarchical optoelectronic device models," in *Languages for System Specification and Verification*, ed. C. Grimm, pp. 145-161, Kluwer, 2004

2. I. O'Connor, F. Gaffiot, "Advanced research in on-chip optical interconnects," in *Low power electronics design*, ed. C. Piguet, CRC press, 2004
3. I. O'Connor, F. Gaffiot, "On-chip optical interconnect for low-power," in *Ultra-low power electronics and design*, ed. E. Macii, Kluwer Academic Publishers, 2004
4. I. O'Connor, F. Tissafi-Drissi, G. Revy, and F. Gaffiot, "UML/XML-based approach to hierarchical AMS synthesis," in *Advances in Specification and Design Languages for SoCs*, ed. A. Vachoux, Kluwer Academic Publishers, 2006
5. J. Gautier, I. O'Connor, "Intégration tridimensionnelle," in *Synthèse de l'année 2007 – Nanocomposants : Les avancées de l'année 2007*, pp. 35-36, ed. S. Fontanell, Observatoire des Micro et NanoTechnologies, 2008
6. I. O'Connor, I. Hassoune, X. Yang, D. Navarro, "Logic circuit design with DGMOS devices," in *Planar Double-Gate Transistor: Technology and Design*, ed. A. Amara, O. Rozeau, Springer, 2009
7. P. Freitas, D. Navarro, I. O'Connor, G. Billiot, H. Lapuyade, J.B. Begueret, "Analog circuits design," in *Planar Double-Gate Transistor: Technology and Design*, ed. A. Amara, O. Rozeau, Springer, 2009
8. I. O'Connor, I. Hassoune, D. Navarro, "Fine-Grain Reconfigurable Logic Cells Based on Double-Gate MOSFETs," in *VLSI-SOC: Design Methodologies for SoC and SiP*, ed. D. Soudris, C. Piguet, R. Reis, Springer, 2009
9. I. O'Connor, "Platform for model-based design of integrated multi-technology systems," in *Model-Based Design for Embedded Systems*, ed. P. Mostermann, G. Nicolescu, CRC Press, 2009
10. I. O'Connor, J. Liu, J. Kotb, N. Yakymets, R. Daviot, D. Navarro, P.E. Gaillardon, F. Clermidy, M. Amadou, G. Nicolescu, "Emerging Technologies and Nanoscale Computing Fabrics," in *VLSI-SOC: Design Methodologies for SoC and SiP*, ed. J. Becker, M. Johann, R. Reis, Springer, 2010
11. L. Gheorghe Iugan, G. Nicolescu, I. O'Connor, "Formalization and validation of an Optical Network-on-Chip using DEVS and timed automata," in *Discrete-Event Modeling and Simulation: Theory and Applications*, ed. G. Wainer, CRC Press, 2010
12. L. Labrak, I. O'Connor, "Multi-physics Optimization Through Abstraction and Refinement," in *Design Technology for Heterogeneous Embedded Systems*, ed. G. Nicolescu, I. O'Connor, C. Piguet, Springer, 2012
13. B. Wang, I. O'Connor, E. Drouard, L. Labrak, "Bottom-up verification for CMOS photonic linear heterogeneous system," in *System Specification and Design Languages*, ed. T. Kazmierski, Springer, 2012
14. A. Allam, I. O'Connor, "A protocol stack architecture for optical network-on-chip: Organization and performance evaluation", in *Integrated Optical Interconnect Architectures and Applications in Embedded Systems*, ed. I. O'Connor, G. Nicolescu, Springer, 2013
15. S. Le Beux, J. Trajkovic, I. O'Connor, G. Nicolescu, G. Bois, P. Paulin, "System Level Exploration for the Integration of Optical Networks on Chip in 3D MPSoC Architectures," in *Integrated Optical Interconnect Architectures and Applications in Embedded Systems*, ed. I. O'Connor, G. Nicolescu, Springer, 2013
16. H. Li, A. Fourmigue, S. Le Beux, X. Letartre, I. O'Connor, G. Nicolescu, "Thermal-Aware Design Method for On-Chip Laser-based Optical Interconnect," in *Optical Interconnects for Computing Systems*, ed. G. Nicolescu, S. Le Beux, M. Nikdast, J. Xu, River Publishers, 2017
17. A. Poittevin, C. Mukherjee, I. O'Connor, C. Maneux, G. Larrieu, M. Deng, S. Le Beux, F. Marc, A. Lecestre, C. Marchand, A. Kumar, "3D Logic Cells Design and Results Based on Vertical NWFET Technology Including Tied Compact Model", in: *VLSI-SoC: Design Trends*, ed. A. Calimera, P.E. Gaillardon, K. Korgaonkar, S. Kvatinsky, R. Reis, IFIP Advances in Information and Communication Technology, vol 621, 2021. Springer, Cham. https://doi.org/10.1007/978-3-030-81641-4_14
18. E. Dupuis, S.I. Filip, O. Sentieys, D. Novo, I. O'Connor, A. Bosio, "Approximations in Deep Learning," in *Approximate Computing Techniques - From Component- to Application-Level*, ed. A. Bosio, D. Menard, O. Sentieys, Springer, 2022 (DOI: 10.1007/978-3-030-94705-7)
19. K. Bresniker, T. Cox, Y. Hayashi, I. O'Connor, H. Kondo, M. Kondo, T. Matsushita, N. Nakano, T. Norikatsu, K. Sano, M. Sato, T. Shimizu, S. Takagi, Y. Yamaguchi, "Systems and Architectures," in *International Roadmap for Devices and Systems™ (IRDS) 2022 Edition*, IEEE, 2022
20. P.A. Matrangolo, C. Marchand, D. Navarro, I. O'Connor, A. Bosio, "Emerging Technologies for Memory-Centric Computing," in *Design and Applications of Emerging Computer Systems*, ed. W. Liu, J. Han, F. Lombardi, Springer, 2024 (DOI: 10.1007/978-3-031-42478-6_1)
21. K. Bresniker, T. Cox, Y. Hayashi, I. O'Connor, H. Kondo, M. Kondo, T. Matsushita, N. Nakano, T. Norikatsu, K. Sano, M. Sato, T. Shimizu, S. Takagi, Y. Yamaguchi, "Systems and Architectures," in *International Roadmap for Devices and Systems™ (IRDS) 2023 Edition*, IEEE, 2023
22. E.T. Breyer, M. Niemier, I. O'Connor, S. Slesazeck, "Logic in memory," in *Ferroelectricity in Doped Hafnium Oxide 2nd edition*, ed. U. Schroeder, C. Seong Hwang, H. Funakubo, Elsevier, 2025

Articles published in refereed publications (journals)

1. F. Gaffiot, K. Vuorinen, F. Mieyeville, I. O'Connor, G. Jacquemod, "Behavioral modeling for hierarchical simulation of optronic systems," *IEEE Transactions on Circuits and Systems - II. Analog and Digital Signal Processing*, vol. 46, no. 10, pp. 1316-1322, October 1999
2. B. Stefanelli, I. O'Connor, L. Quiquerez, A. Kaiser, D. Billet, "An analog beam-forming circuit for ultrasound imaging using switched-current delay lines," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 202-211, February 2000
3. I. O'Connor, A. Kaiser, "Automated synthesis of switched-current cells," *IEEE Transactions on Computer Aided Design*, vol. 19, no. 4, pp. 413-424, April 2000
4. P. Bontoux, I. O'Connor, F. Gaffiot, X. Letartre, G. Jacquemod, "Behavioral modeling and simulation of optical integrated devices," *Special Section of Analog Integrated Circuits and Signal Processing*, vol. 29, issue 1/2, pp. 37-47, October 2001
5. G. Tosik, F. Gaffiot, Z. Lisik, I. O'Connor, F. Tissafi-Drissi, "Power dissipation in optical and metallic clock distribution networks in new VLSI technologies," *Electronics Letters*, vol. 4, no. 3, pp. 198-200, 5 February 2004
6. A. Kazmierczak, M. Brière, E. Drouard, P. Bontoux, P. Rojo-Romeo, I. O'Connor, X. Letartre, F. Gaffiot, R. Orobtchouk, T. Benyattou, "Design, Simulation and Characterization of a Passive Optical Add-Drop Filter in Silicon-On-Insulator Technology," *Photonics Technology Letters*, vol. 17, no. 7, pp. 1447 – 1449, July 2005
7. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Design of a Novel CNTFET-based Reconfigurable Logic Gate," *Electronics Letters*, vol. 43, no. 9, pp. 514-516, 26 April 2007
8. I. O'Connor, F. Tissafi-Drissi, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, J. Van Campenhout, D. Van Thourhout, "Systematic Simulation-Based Predictive Synthesis of Integrated Optical Interconnect," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 8, pp. 927-940, August 2007
9. A. Kazmierczak, E. Drouard, M. Brière, P. Rojo-Romeo, X. Letartre, I. O'Connor, F. Gaffiot, Z. Lisik, "Optimization of an integrated optical crossbar in SOI technology for optical networks on chip," *Journal of Telecommunications and Information Technology*, 3/2007, pp. 109-114, September 2007
10. I. O'Connor, J. Liu, F. Gaffiot, F. Prégaldiny, C. Lallement, C. Maneux, J. Goguet, S. Frégonèse, T. Zimmer, L. Anghel, T. Dang, R. Leveugle, "CNTFET Modeling and Reconfigurable Logic Circuit Design," *IEEE Trans. Circuits and Systems – I. Regular Papers*, vol. 54, no. 11, pp. 2365-2379, November 2007 (DOI: 10.1109/TCSI.2007.907835)
11. I. Hassoune, I. O'Connor, "Double-Gate MOSFET Based Reconfigurable Cells," *Electronics Letters*, vol. 43, no. 23, pp. 1273-1274, 8 November 2007
12. I. Hassoune, X. Yang, I. O'Connor, D. Navarro, "Ultra-Low Power Full Adder Circuit Using SOI Double-Gate MOSFET Devices," *Electronics Letters*, vol. 44, no. 18, pp. 1095-1096, 28 August 2008
13. I. O'Connor, J. Liu, D. Navarro, R. Daviot, N. Abouchi, P.E. Gaillardon, F. Clermidy, "Molecular electronics and reconfigurable logic," *Int. J. Nanotechnology*, vol. 7, nos. 4/5/6/7/8, pp. 367-382, 2010
14. I. Hassoune, D. Flandre, I. O'Connor, J.D. Legat, "ULPFA: a new efficient design of a power aware full adder," *IEEE Trans. Circuits and Systems – I. Regular Papers*, vol. 57, no. 8, pp. 2066–2074, Aug. 2010
15. S. Le Beux, J. Trajkovic, I. O'Connor, G. Nicolescu, G. Bois, P. Paulin, "Multi-Optical Network on Chip for Large Scale MPSoC", *IEEE Embedded Systems Letters*, vol. 2, no. 3, pp. 77-80, September 2010
16. I. O'Connor (Guest Editor), "Introduction to the special issue on TAISA 2007," *Analog Integrated Circuits and Signal Processing*, vol. 65, no. 3, pp. 343-344, December 2010
17. P.E. Gaillardon, F. Clermidy, I. O'Connor, J. Liu, R. Daviot, N. Abouchi, M. Amadou, G. Nicolescu, "Matrix Nanodevice-Based Architectures and Associated Functional Mapping Method," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 7, no. 1, January 2011
18. M.H. Ben-Jamaa, P.E. Gaillardon, F. Clermidy, I. O'Connor, D. Sacchetto, G. De Micheli, Y. Leblebici, "Silicon Nanowire Arrays and Crossbars: Top-Down Fabrication Techniques and Circuit Applications," *ASP Science of Advanced Materials (SAM)*, *Special Issue on "Nano-Engineered Silicon: Technology and Applications"*, vol. 3, p. 466–476, 2011
19. M. H. Ben Jamaa, P.E. Gaillardon, S. Frégonèse, M. De Marchi, G. De Micheli, T. Zimmer, I. O'Connor, F. Clermidy, "FPGA Design with Double-Gate Carbon Nanotube Transistors," *ECS Transactions - CSTIC 2011 "Emerging Semiconductor Technologies"*, vol. 34, March 2011

20. R. Dahmani, O. Valorge, F. Sun, S. Labiod, F. Calmon, S. Latreche, I. O'Connor; C. Gontrand, "Insights into Three-Dimensional Radiofrequency Circuits Connections", *Journal of Computer Technology and Application*, vol. 2, pp. 456-470, 2011
21. W. Du, D. Navarro, F. Mieyeville, I. O'Connor, "IDEA1: A Validated SystemC-based System-level Design and Simulation Environment for Wireless Sensor Networks," *EURASIP Journal on Wireless Communications and Networking* (DOI: 10.1186/1687-1499-2011-143, October 2011)
22. F. Yengui, L. Labrak, F. Frantz, R. Daviot, N. Abouchi, I. O'Connor, "A hybrid GA–SQP algorithm for analog circuits sizing," *Scientific Research Circuits and Systems Journal*, vol. 3, no. 2, pp. 146-152, April 2012 (DOI: 10.4236/cs.2012.32019)
23. F. Frantz, L. Labrak, I. O'Connor, "3D IC floorplanning: automating optimization settings and exploring new thermal-aware management techniques," *Elsevier Microelectronics Journal*, vol. 43, no. 6, pp. 423-432, June 2012
24. H. Filiol, I. O'Connor, D. Morche, "Analog IC variability bound estimation using the Cornish-Fisher expansion", *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 9, pp. 1457-1461, Sept. 2012
25. P.E. Gaillardon, D. Sacchetto, G. Beneventi, M. H. Ben Jamaa, L. Perniola, F. Clermidy, I. O'Connor, G. De Micheli, "Design and Architectural Assessment of 3-D Resistive Memory Technologies in FPGAs," *IEEE Trans. Nanotechnology*, vol. 12, no. 1, pp. 40-50, Jan. 2013
26. S. Le Beux, I. O'Connor, G. Nicolescu, G. Bois, P. Paulin, "Reduction methods for adapting optical network on chip topologies to 3D architectures," *Elsevier Microprocessors and Microsystems - Embedded Hardware Design*, vol. 37, no. 1, pp. 87-98, Feb. 2013
27. M. Galos, F. Mieyeville, D. Navarro, I. O'Connor, "SystemC fine-grained HW–SW fully heterogeneous WSN simulation and UML metamodel behavioural extraction," *Analog Integrated Circuits and Signal Processing*, vol. 77, no. 2, pp. 123-133, Sept. 2013
28. N. Zhu, I. O'Connor, "iMASKO: A Genetic Algorithm Based Optimization Framework for Wireless Sensor Networks," *J. Sensor and Actuator Networks*, vol. 2, no. 4, pp. 675-699, Oct. 2013 (DOI: 10.3390/jsan2040675)
29. D. Navarro, Z. Feng, I. O'Connor, "Image Toolbox for CMOS Image Sensors Fast Simulation," *Global Journal of Computer Science and Technology – Graphics & Vision*, vol. 13, no. 3, 2013
30. K. Jabeur, I. O'Connor, N. Yakymets, "Functions classification approach to generate reconfigurable fine-grain logic based on Ambipolar Independent Double Gate FET (Am-IDGFET)," *Elsevier Microelectronics Journal*, vol. 44, no. 12, pp. 1316-1327, Dec. 2013 (DOI: 10.1016/j.mejo.2013.09.001)
31. C. Baudot, J.M. Fédéli, D. Marris-Morini, B. Caire-Remonnay, L. Virot, S. Olivier, A. Myko, P. Grosse, G. Grand, B. Ben Bakir, J.M. Hartmann, N. Allouti, S. Barnola, C. Vizioz, M. Rivoire, A. Seignard, N. Vulliet, A. Souhaité, S. Messaoudène, I. O'Connor, L. Vivien, S. Menezo, F. Boeuf, "Introducing photonic devices for 40Gbits/s wavelength division multiplexing transceivers on 300-mm SOI wafers using CMOS processes," Integrated Optics: Devices, Materials, and Technologies XVIII, ed. J.E. Broquin, G. Nunzi Conti, Proc. SPIE, vol. 8988, pp. 89880O-1 – 89880O-16, Mar. 2014 (DOI: 10.1117/12.2042496)
32. S. Le Beux, H. Li, G. Nicolescu, J. Trajkovic, I. O'Connor, "Optical Crossbars on Chip, A Comparative Study based on Worst-Case Losses," in *Wiley Concurrency and Computation: Practice and Experience (CCPE)*, Special Issue on Silicon Photonics, pp.2492-250, 2014 (DOI: 10.1002/cpe.3336)
33. W. Du, F. Mieyeville, D. Navarro, I. O'Connor, L. Carrel, "Modeling and simulation of networked low-power embedded systems: a taxonomy," *EURASIP Journal on Wireless Communications and Networking*, 2014:106, Jul. 2014 (DOI: 10.1186/1687-1499-2014-106)
34. P.E. Gaillardon, G. De Micheli, I. O'Connor, S. Mitra, T. Ernst, "Introduction to the special section on functionality-enhanced devices", *IEEE Trans. Nanotechnology*, vol. 13, no. 6, p. 1019, Nov. 2014 (DOI: 10.1109/TNANO.2014.2360284)
35. K. Jabeur, I. O'Connor, S. Le Beux, "Ambipolar Independent Double Gate FET (Am-IDGFET) for the Design of Compact Logic Structures," *IEEE Trans. Nanotechnology*, vol. 13, no. 6, pp. 1063-1073, Nov. 2014 (DOI: 10.1109/TNANO.2014.2306071)
36. J.E. Lorival, F. Calmon, F. Sun, F. Frantz, C. Plossu, M. LeBerre, I. O'Connor, O. Valorge, J. Charbonnier, D. Henry, C. Gontrand, "An efficient and simple compact modeling approach for 3-D interconnects with IC's stack global electrical context consideration," *Microelectronics Journal*, vol. 46, no. 1, pp.153–165, Jan. 2015 (DOI: 10.1016/j.mejo.2014.12.002)
37. N. Yakymets, I. O'Connor, K. Jabeur, S. Le Beux, "Multi-Level Mapping of Nanocomputer Architectures Based on Hardware Reuse," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, Special Issue

on Computing in Emerging Technologies, vol. 5, no. 1, pp. 88-97, Mar. 2015 (DOI: 10.1109/JETCAS.2014.2374272)

38. O. Dubray, A. Abraham, K. Hassan, S. Olivier, D. Marris-Morini, L. Vivien, I. O'Connor, S. Menezo, "Electro-optical ring modulator: an ultra-compact model for the comparison and optimization of PN, PIN, and capacitive junction," *IEEE J. Selected Topics in Quantum Electronics*, 2016, vol. 22, no. 6, Nov-Dec 2016 (DOI: 10.1109/JSTQE.2016.2564103)
39. H. Li, S. Le Beux, M.J. Sepulveda Florez, I. O'Connor, "Energy-Efficiency Comparison of Multi-Layer Deposited Nanophotonic Crossbar Interconnects," *ACM J. Emerging Technologies in Computing Systems*, Association for Computing Machinery, vol. 20, Jul. 2017 (DOI: 10.1145/3094125)
40. S. Le Beux, P.V. Gratz, I. O'Connor, "Guest Editorial: Emerging Technologies and Architectures for Manycore Computing Part 1: Hardware Techniques," IEEE Trans. Multi-Scale Computing Systems, vol. 4, no. 2, pp. 97-98, Apr-Jun 2018 (DOI: 10.1109/TMSCS.2018.2826758)
41. J. Luo, C. Killian, S. Le Beux, D. Chillet, O. Sentieys, I. O'Connor, "Offline optimization of wavelength allocation and laser power in nanophotonic interconnects," ACM J. Emerging Technologies in Computing Systems (JETC), vol. 14, no. 2, Jul. 2018 (DOI: 10.1145/3178453)
42. H. Li, A. Fourmigue, S. Le Beux, I. O'Connor, G. Nicolescu, "Towards maximum energy efficiency in nanophotonic interconnects with thermal-aware on-chip laser tuning," *IEEE Trans. Emerging Topics in Computing*, vol. 6, no. 3, pp. 343-356, Jul. – Sep. 2018 (DOI: 10.1109/TETC.2016.2561623)
43. Q. An, S. Le Beux, I. O'Connor, J.O. Klein, "A comprehensive compact model for the design of all-spin-logic based circuits," Microelectronics Journal, Nov. 2018 (DOI: 10.1016/j.mejo.2018.11.003)
44. A. Levisse, P.E. Gaillardon, B. Giraud, I. O'Connor, J.P. Noel, M. Moreau, J.M. Portal, "Resistive Switching Memory Architecture Based on Polarity Controllable Selectors," IEEE Trans. Nanotechnology, vol. 18, pp. 183-194, 2019 (DOI: 10.1109/TNANO.2018.2887140)
45. Y. Wang, A. Aouina, H. Li, I. O'Connor, G. Nicolescu, S. Le Beux, "Thermal-Aware Design Method for Laser Group Control in Nanophotonic Interconnects," IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol. 27, no. 3, pp. 742-746, Mar. 2019 (DOI: 10.1109/TVLSI.2018.2888589)
46. E. Fusella, M. Nikdast, I. O'Connor, J. Flich, S. Pasricha, "Guest Editors' Introduction: Emerging Networks-on-Chip – Designs, Technologies, and Applications," ACM J. Emerging Technologies in Computing Systems, 2019 (DOI: 10.1145/3296021)
47. A. Perodou, A. Korniienko, G. Scorletti, M. Zarudniev, J.B. David, I. O'Connor, "Frequency Design of Lossless Passive Electronic Filters: a state-space formulation of the direct synthesis approach," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 1, Jan. 2021 (DOI: 10.1109/TCSI.2020.3034300)
48. E. Dupuis, D. Novo, I. O'Connor, A. Bosio, "CNN weight sharing based on a fast accuracy estimation metric," *Microelectronics Reliability*, 122(12):114148, July 2021 (DOI: 10.1016/j.microrel.2021.114148)
49. F. Fummi, I. O'Connor, "Holding Conferences Online in Pandemic Times: The DATE Experience," *IEEE Design & Test*, vol. 38, no. 4, pp. 128-130, August 2021 (DOI: 10.1109/MDAT.2021.3078673)
50. C. Mukherjee, A. Poittevin, I. O'Connor, G. Larrieu, C. Maneux, "Compact modeling of 3D vertical junctionless gate-all-around silicon nanowire transistors towards 3D logic design," *Solid-State Electronics*, 183(9):108125, September 2021 (DOI: 10.1016/j.sse.2021.108125)
51. A. Ruospo, E. Sanchez, M. Traiola, I. O'Connor, A Bosio, "Investigating data representation for efficient and reliable Convolutional Neural Networks," *Microprocessors and Microsystems*, vol. 86, 104318, October 2021 (DOI: 10.1016/j.micpro.2021.104318)
52. C. Marchand, I. O'Connor, M. Cantan, S. Slesazeck, T. Mikolajick, "A FeFET-based hybrid memory accessible by content and by address," *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits*, vol. 8, no. 1, pp. 19-26, June 2022 (DOI: 10.1109/JXCDC.2022.3168057)
53. M. Abdalla, C. Zrounba, R. Cardoso, P. Jimenez, G. Ren, A. Boes, A. Mitchell, A. Bosio, I. O'Connor, F. Pavanello, "Minimum complexity integrated photonic architecture for delay-based reservoir computing," *Optics Express*, 31(7), pp. 11610-11623, 2023 (DOI: 10.1364/OE.484052)
54. C. Cakirlar, M. Simon, G. Galderisi, I. O'Connor, T. Mikolajick, J. Trommer, "Cross-Shape Reconfigurable Field Effect Transistor for Flexible Signal Routing," *Materials Today Electronics*, vol. 4, June 2023, 100040 (DOI: 10.1016/j.mtelec.2023.100040)
55. I. O'Connor, R. Wille, A. Pimentel, V. Bertacco, "Post-Pandemic Conferences: The DATE Experience," *IEEE Design & Test*, vol. 40, no. 5, pp. 104-112, October 2023 (DOI: 10.1109/MDAT.2023.3287930)

56. S. Mannaa, A. Poittevin, C. Marchand, D. Deleruyelle, B. Deveautour, A. Bosio, I. O'Connor, C. Mukherjee, Y. Wang, H. Rezgui, M. Deng, C. Maneux, J. Müller, S. Pelloquin, K. Moustakas, G. Larrieu, "3D Logic circuit design oriented electrothermal modeling of vertical junctionless nanowire FETs," *IEEE J. Exploratory Solid-State Computational Devices and Circuits*, vol. 9, no. 2, pp. 116-123, Dec. 2023 (DOI: 10.1109/JXCDC.2023.3309502)
57. A. Ram, K. Maity, C. Marchand, A. Mahmoudi, A.R. Kshirsagar, M. Soliman, T. Taniguchi, K. Watanabe, B. Doudin, A. Ouerghi, S. Reichardt, I. O'Connor, J.F. Dayen, "Reconfigurable Multifunctional van der Waals Ferroelectric Devices and Logic Circuits," *ACS Nano*, October 2023 (DOI: 10.1021/acsnano.3c07952)
58. R. Cardoso, C. Zrounba, M. Abdalla, M. Gomes de Queiroz, P. Jimenez, I. O'Connor, S. Le Beux, "Reconfigurable Photonic GEMM Based on Phase-Change-Materials and Stochastic Computing," *IEEE/Optica J. Lightwave Technology*, July 2024 (DOI: 10.1109/JLT.2024.3421621)
59. M. Abdalla, R. Cardoso, P. Jimenez, M. Gomes de Queiroz, A. Boes, G. Ren, A. Mitchell, I. O'Connor, F. Pavanello, "Mask-less asynchronous time-delay reservoir computing using a passive photonic integrated circuit," *Journal of Lightwave Technology*, July 2024 (DOI: 10.1109/JLT.2024.3434538)
60. M. Gomes de Queiroz, P. Jimenez, R. Cardoso, M. Vidaletti da Costa, M. Abdalla, I. O'Connor, A. Bosio, F. Pavanello, "The Impact of Feature Representation on the Accuracy of Photonic Neural Networks," *APL Machine Learning*, September 2024 (DOI: 10.1063/5.0226172)
61. S. Saeedi, A. Piri, B. Deveautour, I. O'Connor, A. Bosio, A. Savino, S. Di Carlo, "A Survey on Design Space Exploration Approaches for Approximate Computing Systems," *Electronics*, 13(22), 4442, October 2024 (DOI: 10.3390/electronics13224442)
62. M. Soliman, C. Marchand, A. Mahmoudi, N. Kumar Rajak, T. Taniguchi, K. Watanabe, A. Gloppe, B. Doudin, D. Deleruyelle, I. O'Connor, A. Ouerghi, J.F. Dayen, "Van der Waals Inverted-Floating-Gate Transistors for Artificial Intelligence Electronics," *ACS Nano 2025*, 19(19), 18757–18768, May 2025 (DOI: 10.1021/acsnano.5c03875)
63. J.P. Martinez, N. Bhattacharjee, Y. He, G. Galderisi, B. Sapui, S. Mannaa, I. O'Connor, V. Sessi, P. Javorka, T. Mikolajick, J. Trommer, "Efficient In-Hardware Matrix–Vector Multiplication and Addition Exploiting Bilinearity of Schottky Barrier Transistors Processed on Industrial FDSOI," *Advanced Electronic Materials*, p. e00864, April 2026 (DOI: 10.1002/aelm.202500864)
64. A. Karim, B. Darne, P.A. Matrangolo, J. Falk, I. O'Connor, C. Marchand, A. Bosio, J. Teich, "FeMFET-based high-performance, ultra-low power memory cells for reliable state retention of dataflow networks," Microprocessors and Microsystems, 105303, June 2026 (DOI: 10.1016/j.micpro.2026.105303)
65. J. Trommer, G. Galderisi, J.P. Martinez, Y. He, K. Pingen, L. Tellis, C. Cakirlar, C. Beyer, B. Sapui, E.S. Oliveros-Mata, A. Kumar, J. Knoch, K. Hofmann, S. Carrara, E. Cantatore, M. Lemme, I. O'Connor, A. Heinzig, T. Mikolajick, W.M. Weber, "Re-Thinking Electronic Circuit Design Through Emerging Reconfigurable Field Effect Transistors," *Advanced Science*, published online October 2026 (DOI: 10.1002/advs.78121)
66. C. Cakirlar, T. Obukhova, O. Baumgartner, M. Thesberg, J.M. Gonzalez-Medina, S. Mannaa, I. O'Connor, T. Mikolajick, D. Deleruyelle, J. Trommer, "Electrostatics of Common-Channel RFETs: From X-Shape to U-Shape," *physica status solidi (a) applications and materials science*, published online 2026 (DOI: 10.1002/pssa.70567)

Invited articles published in refereed international conference proceedings

1. I. O'Connor, "EDA Tools and Methods for Synthesis of Analog, Mixed-Signal and Mixed-Domain Integrated Systems," *Summer School of Microelectronics*, Lodz (Poland), 25-28 Sept. 2002
2. I. O'Connor, "Interconnexions optiques intégrées pour les systèmes sur puce," *Microsystèmes à cœur optique*, Marseille, 5 Feb. 2004
3. I. O'Connor, "Invited Talk: Optical solutions for system-level interconnect," *System-Level Interconnect Prediction*, pp. 79-88, Paris, France 14-15 February 2004
4. C. Piguet, J. Gautier, C. Heer, I. O'Connor, U. Schlichtmann, "Extremely Low-Power Logic," *Design Automation and Test in Europe*, pp. 656-661, Paris, France, 16-20 February 2004
5. I. O'Connor, M. Brière, E. Drouard, A. Kazmierczak, F. Tissafi-Drissi, D. Navarro, F. Mieyeville, J. Dambre, D. Stroobandt, J.M. Fedeli, Z. Lisik, F. Gaffiot, "Towards reconfigurable optical networks on chip," *Reconfigurable Communication centric SoCs*, *Montpellier*, France, 27-29 June 2005
6. F. Gaffiot, M. Brière, E. Drouard, A. Kazmierczak, D. Navarro, F. Mieyeville, G. Tosik, Z. Lisik, I. O'Connor, "Network on Chip: An Optical Alternative?" *Multiconference on Systemics*, *Cybernetics and Informatics*, Orlando, Florida, USA, 10-13 July 2005

7. I. O'Connor, F. Tissafi-Drissi, D. Navarro, F. Mieyeville, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, M. Brière, "Integrated optical interconnect for on-chip data transport," *IEEE-NEWCAS Conference*, June 18-21, 2006, Gatineau, Canada
8. I. O'Connor, J. Liu, F. Gaffiot, "CNTFET-based logic circuit design," *IEEE Int. Conf. Design & Test of Integrated Systems in Nanoscale Technology*, Tunis, Tunisia, 5-7 Sept. 2006
9. I. O'Connor, B. Courtois, K. Chakrabarty, N. Delorme, M. Hampton, J. Hartung, "Heterogeneous Systems on Chip and Systems in Package," *Design Automation and Test in Europe*, Nice, France, 16-20 April 2007
10. I. O'Connor, H. Charlery, "Synthesis of physically heterogeneous systems on chip," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 634-637
11. I. O'Connor, J. Liu, D. Navarro, I. Hassoune, S. Burignat, F. Gaffiot, "Ultra-Fine Grain reconfigurability Using CNTFETs," *IEEE International Conference on Electronics, Circuits and Systems*, 11-14 December 2007, Marrakech, Morocco
12. I. O'Connor, J. Liu, D. Navarro, F. Gaffiot, "Dynamically Reconfigurable Logic Gate Cells and Matrices using CNTFETs," *IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era*, 26-28 March 2008, Tozeur, Tunisia
13. F. Gaffiot, I. O'Connor, "Integrated optical interconnects: what could be possible?" Keynote, *12th IEEE Workshop on Signal Propagation on Interconnects*, 12-15 May 2008, Avignon, France
14. I. O'Connor, F. Mieyeville, F. Gaffiot, A. Scandurra, G. Nicolescu, "Can integrated photonics solve MPSoC interconnect issues?" *Int. VLSI/ULSI Multilevel Interconnection Conference*, 27-30 October 2008, Fremont (CA), USA
15. D. Van Thourhout, I. O'Connor, A. Scandurra, L. Liu, W. Bogaerts, S. Selvaraja, "Nanophotonic Devices for Optical Networks-On-Chip," *Conference on Lasers and Electro-Optics (CLEO)*, May 31 – June 5, 2009, Baltimore (MD), USA
16. S. Le Beux, G. Nicolescu, I. O'Connor, "System-Level Exploration for 3D MPSoCs including Optical Networks-on-Chip," *MPSoC 2009*, Savannah (GA), USA, 2-7 August 2009
17. I. O'Connor, "Emerging technologies and nanoscale computing fabrics," Keynote, *17th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 12-14 2009, Florianopolis, Brazil
18. L. Labrak, I. O'Connor, "Heterogeneous System Design Platform and Perspectives for 3D Integration," *International Conference on Microelectronics (ICM)*, 19-22 December 2009, Marrakech, Morocco
19. M. Amadou, S. Le Beux, G. Nicolescu, I. O'Connor, "Functional Mapping for Nanodevice-Based Architectures," *International Conference on Microelectronics (ICM)*, 19-22 December 2009, Marrakech, Morocco
20. A. Allam, I. O'Connor, A. Scandurra, "Optical Network-on-Chip Reconfigurable Model for Multi-Level Analysis," *International Symposium on Circuits and Systems (ISCAS)*, 30 May-2 June 2010, Paris, France
21. I. O'Connor, "Optical networks on chip for MPSoC data communication," *International Forum on Embedded MPSoC and Multicore (MPSoC)*, 28 June-2 July 2010, Gifu, Japan
22. F. Mandorlo, C. Sciancalepore, I. O'Connor, P. Rojo Romeo, C. Seassal, P. Viktorovitch, X. Letartre, B. Ben Bakir, D. Bordel, N. Olivier, J.M. Fedeli, "Heterogeneous Integration of III-V Lasers on Silicon for Photonic/Electronic Convergence," *IEEE Winter Topical Meetings - Photonic Materials and Integration Architectures*, 10-12 January 2011, Keystone (CO), USA
23. I. O'Connor, K. Jabeur, S. Le Beux, D. Navarro, N. Yakymets, P.E. Gaillardon, M.H. Ben Jamaa, F. Clermidy, "Nanofabrics for reconfigurable computing cores," *Int. Forum on Embedded MPSoC and Multicore (MPSoC)*, Beaune, France, July 4-8 2011
24. S. Le Beux, J. Trajkovic, I. O'Connor, G. Nicolescu, "Layout Guidelines for 3D Architectures including Optical Ring Network-on-Chip (ORNoC)," *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Hong Kong, China, 3-5 October 2011
25. I. O'Connor, D. Van Thourhout, A. Scandurra," Wavelength Division Multiplexed Photonic Layer on CMOS," *6th International Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC)*, Paris, France, 23-25 January 2012
26. I. O'Connor, K. Jabeur, S. Le Beux, D. Navarro, "Ambipolar Independent Double Gate FET Logic," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, Amsterdam, Netherlands, 4-6 July 2012
27. S. Le Beux, I. O'Connor, Z. Li, X. Letartre, C. Monat, J. Trajkovic, G. Nicolescu, "Potential and pitfalls of silicon photonics computing and interconnect," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, 19–23 May 2013

28. I. O'Connor, "New Computing Paradigms with Emerging Technologies," *14ème Journées Nano, Micro et Optoélectronique (JNMO)*, Evian, France, 21-23 May 2013
29. S. Le Beux, Z. Li, C. Monat, X. Letartre, I. O'Connor, "Reconfigurable photonic switching: Towards all-optical FPGAs," *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 180-185, Istanbul, Turkey, 7-9 October 2013
30. I. O'Connor, "From performance modeling to design space modeling: an exploration method for heterogeneous systems," *Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes (FETCH)*, Ottawa, Canada, 8-10 January 2014
31. S. Le Beux, H. Li, K. Cheshmi, X. Liu, J. Trajkovic, G. Nicolescu, I. O'Connor, "Optical Crossbars on Chip, a comparative study based on worst-case propagation losses," *Workshop on Exploiting Silicon Photonics for energy-efficient heterogeneous parallel architectures, Conference on High Performance and Embedded Architecture and Compilation (HIPEAC)*, Vienna, Austria, 20-22 January 2014
32. S. Le Beux, H. Li, I. O'Connor, K. Cheshmi, X. Liu, J. Trajkovic, G. Nicolescu, "CHAMELEON: CHANNEL Efficient Optical Network-on-Chip," *Design Automation and Test in Europe (DATE)*, Dresden, Germany, 24-28 March 2014 (DOI: 10.7873/DATE.2014.317)
33. S. Le Beux, H. Li, G. Nicolescu, I. O'Connor, "A Reconfigurable Optical Network on Chip for Streaming Applications," *9th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, Montpellier, France 26-28 May 2014 (DOI: 10.1109/ReCoSoC.2014.6861340)
34. I. O'Connor, "Emerging technologies and nanoscale computing fabrics," *CMOS Emerging Technologies Research Symposium, Grenoble*, France, 6-8 July, 2014
35. Z. Li, S. Le Beux, C. Monat, X. Letartre, I. O'Connor, "Multilevel Modeling Methodology for Reconfigurable Computing Systems Based on Silicon Photonics," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 561-566, Montpellier, France, 8-10 July 2015 (DOI: 10.1109/ISVLSI.2015.129)
36. A. Aziz, E.T. Breyer, A. Chen, X. Chen, S. Datta, S.K. Gupta, M. Hoffmann, X.S. Hu, A. Ionescu, M. Jerry, T. Mikolajick, H. Mulaosmanovic, K. Ni, M. Niemier, I. O'Connor, A. Saha, S. Slesazeck, S.K. Thirumala, X. Yin, "Computing with ferroelectric FETs: Devices, models, systems, and applications," *Design, Automation and Test in Europe (DATE)*, Dresden, Germany, 19-23 March 2018 (DOI: 10.23919/DATE.2018.8342213)
37. I. O'Connor, M. Cantan, C. Marchand, B. Vilquin, S. Slesazeck, E.T. Breyer, H. Mulaosmanovic, B. Giraud, J.P. Noël, A. Ionescu, I. Stolichnov, "Prospects for energy-efficient edge computing with integrated HfO_2-based ferroelectric devices," *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Verona, Italy, 8-10 October 2018 (DOI: 10.1109/VLSI-SoC.2018.8644809)
38. J. Luo, V.D. Pham, C. Killian, D. Chillet, I. O'Connor, O. Sentieys, S. Le Beux, "Run-Time management of energy-performance trade-off in Optical Network-on-Chip," *IEEE Conference on Design of Circuits and Integrated Systems*, Lyon, France, 14-16 November 2018 (DOI: 10.1109/DCIS.2018.8681477)
39. A. Bosio, I. O'Connor, G. Rodrigues, F. Lima, E.I. Vatajelu, G. Di Natale, L. Anghel, S. Nagarajan, M. Fieback, S. Hamdioui, "Rebooting Computing: The Challenges for Test and Reliability," *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, Delft, Netherlands, 2-4 October 2019 (DOI: 10.1109/DFT.2019.8875270)
40. David Brooks, Martin M. Frank, Tayfun Gokmen, Udit Gupta, X. Sharon Hu, Shubham Jain, Ann Franchesca Laguna, Michael Niemier, Ian O'Connor, Anand Raghunathan, Ashish Ranjan, Dayane Reis, Jacob R. Stevens, Carole-Jean Wu, Xunzhao Yin, "Emerging Neural Workloads and Their Impact on Hardware," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Grenoble, France, 9-13 March 2020 (DOI: 10.23919/DATE48585.2020.9116435)
41. A. Bosio, M. Cantan, C. Marchand, I. O'Connor, P. Fiser, A. Poittevin, M. Traiola, "Emerging Technologies: Challenges and Opportunities for Logic Synthesis," *International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, p. 93-98, Vienna, Austria, 7-9 April 2021 (DOI: 10.1109/DDECS52668.2021.9417062)
42. I. O'Connor, D. Atienza, J. Trommer, O. Baumgartner, G. Larrieu, C. Maneux, "3D compute cubes for edge intelligence: nanoelectronic-enabled adaptive systems based on junctionless, ambipolar, and ferroelectric vertical FETs," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium (virtual), 14-23 March 2022
43. C. Zrounba, F. Bentata, R. Cardoso, A. Bosio, S. Le Beux, P. Genevet, S. Monfray, L. Berguiga, I. O'Connor, S. Cueff, F. Pavanello, "Simulation-based Comparison of the Performance of Various Phase-Change Materials on a SiN-

based Photonic Platform", *Metamaterials, Photonic Crystals and Plasmonics (META 2022)*, Torremolinos, Spain, 19-22 July 2022

44. M. Niemier, X.S. Hu, L. Liu, M. Sharifi, I. O'Connor, D. Atienza, G. Ansaloni, C. Li, A. Khan, D. Ralph, "Cross Layer Design for the Predictive Assessment of Technology-Enabled Architectures," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, 17-19 April 2023 (DOI: 10.23919/DATE56975.2023.10136923)
45. S. Mannaa, C. Marchand, D. Deleruyelle, B. Deveautour, I. O'Connor, A. Bosio, "VNWFET-based technology: from device modelling to standard cell library," *IEEE Int. Conf. Nanotechnology (NANO)*, Jeju, South Korea, 2-5 July 2023 (DOI: 10.1109/NANO58406.2023.10231288)
46. C. Marchand, A. Nicolas, P.A. Matrangolo, D. Navarro, A. Bosio, I. O'Connor, "FeFET based Logic-in-Memory design methodologies, tools and open challenges," *31st IFIP/IEEE Conference on Very Large Scale Integration (VLSI-SoC)*, Dubai, UAE, 16-18 October 2023 (DOI:10.1109/VLSI-SoC57769.2023.10321901)
47. A.F. Laguna, M.M. Sharifi, D. Reis, L. Liu, A. Hennessee, C. O'Dell, I. O'Connor, M. Niemier, X.S. Hu, "Invited Paper: Algorithm/Hardware Co-design for Few-Shot Learning at the Edge" (invited), *IEEE/ACM Int. Conf. Computer Aided Design (ICCAD)*, San Francisco (CA), USA, 29 October - 2 November 2023 (DOI: 10.1109/ICCAD57390.2023.10323933)
48. R. Bishnoi, S. Diware, A. Gebregiorgis, S. Thomann, S. Mannaa, B. Deveautour, C. Marchand, A. Bosio, D. Deleruyelle, I. O'Connor, H. Amrouch, S. Hamdioui, "Energy-Efficient Computation-In-Memory Architecture Using Emerging Technologies," *IEEE International Conference on Microelectronics (ICM)*, Abu Dhabi, UAE, 17-20 December 2023 (DOI: 10.1109/ICM60448.2023.10378889)
49. M. Niemier, M. Sharifi, Z. Enciso, I. O'Connor, P. Gupta, J. Castrillon, J. Lima, J. Ryckaert, "Smoothing Disruption Across the Stack: Tales of Memory, Heterogeneity, & Compilers," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Valencia, Spain, 25-27 March 2024 (DOI: 10.23919/DATE58400.2024.10546772)
50. S. Mannaa, P.A. Matrangolo, C. Marchand, D. Deleruyelle, B. Deveautour, I. O'Connor, A. Bosio, "VNWFET-based Systolic Array accelerator for Deep Neural Networks," *2024 IEEE 24th International Conference on Nanotechnology (NANO)*, Gijón, Spain, July 8-11, 2024 (DOI: 10.1109/NANO61778.2024.10628674)
51. L. Krupp, I. O'Connor, L. Benini, X.S. Hu, J. Rodrigues, C. Studer, N. Wehn, "Improving Chip Design Enablement for Universities in Europe – A Position Paper," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Lyon, France, 31 March – 2 April 2025 (DOI: 10.23919/DATE64628.2025.10992734)
52. B. Darne, A. Karim, P.A. Matrangolo, J. Falk, I. O'Connor, C. Marchand, A. Bosio, J. Teich, "FeMFET-based High Performance, Ultra-Low Power Memory Cells for Reliable State Retention of Dataflow Networks," *IEEE Int. Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)*, Barcelona, Spain, 21-23 October 2025

Articles published in refereed international conference proceedings

1. I. O'Connor, A. Kaiser, "Automated design of switched-current cells," *Proc. Custom Integrated Circuits Conference*, pp. 477-480, Santa-Clara (USA), May 1998
2. B. Stefanelli, I. O'Connor, L. Quiquerez, A. Kaiser, D. Billet, "An analog beam-forming circuit using switched-current delay lines," *Proc. European Solid-State Circuits Conference*, pp. 300-303, The Hague (Netherlands), Sep. 1998
3. P. Bontoux, I. O'Connor, F. Gaffiot, G. Jacquemod, "Design and optimization of passive components for optical interconnects," *DTIP'2000*, Paris, May 9-11, 2000
4. P. Bontoux, F. Mieyeville, I. O'Connor, F. Gaffiot, G. Jacquemod, "Design and optimization of optical links based on VHDL-AMS modeling," *BMAS'2000*, Orlando, FL, USA, October 19-20, 2000, p.62-67
5. F. Mieyeville, G. Jacquemod, I. O'Connor, F. Gaffiot, "Behavioral modeling of short distance optical interconnects," *ISMA 2000*, Singapore, 27 November-2 December 2000, SPIE Proceedings vol. 4228, n° 02, pp. 1-8
6. I. O'Connor, F. Mieyeville, F. Tissafi-Drissi, F. Gaffiot, "Exploration paramétrique d'amplificateurs de transimpédance CMOS à bande passante maximisée," *Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications*, Paris, France, Sept. 2002
7. F. Mieyeville, F. Gaffiot, I. O'Connor, J. Oudinot, P. Raynaud, F Mkalech, "VCSEL-based Optical Communication Link Simulation using VHDL-AMS," *DATE 2003*, Exhibition forum, Session X

8. M. Brière, F. Gaffiot, I. O'Connor, L. Carrel, "Integration of an FDTD algorithm in an electronic design framework," *5th International Workshop on Computational Electromagnetics*, pp. 21-26, Halifax, Canada, 17-19 June 2003
9. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, F. Gaffiot, "Design methodologies for high-speed CMOS photoreceiver front-ends," *16th Symposium On Integrated Circuits And System Design*, pp. 323-328, Sao Paolo, Brazil, 8-11 September 2003
10. G. Tosik, F. Gaffiot, Z. Lisik, I. O'Connor, F. Tissafi-Drissi, "Optical versus metallic interconnections for clock distribution networks in new VLSI technologies," *13th International Workshop on Power and Timing Modeling, Optimization and Simulation*, PATMOS 2003, pp. 461-470, Torino, Italy, 10-12 September 2003
11. G. Tosik, F. Gaffiot, Z. Lisik, I. O'Connor, "Optical versus Electrical Clock System in Future VLSI Technologies," *IEEE International SOC Conference*, pp. 261-262, Portland, USA, 17-20 September 2003
12. F. Mieyeville, M. Brière, I. O'Connor, F. Gaffiot, G. Jacquemod, "A VHDL-AMS library of hierarchical optoelectronic device models," *Forum on Specification and Design Languages*, pp. 7-18, Frankfurt, Germany, 23-26 September 2003
13. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, F. Gaffiot, "Hierarchical synthesis of high-speed CMOS photoreceiver front-ends using a multi-domain behavioral description language," *Forum on Specification and Design Languages*, pp. 151-162, Frankfurt, Germany, 23-26 September 2003
14. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, G. Tosik, F. Gaffiot, "Méthodologie de conception d'un photo-récepteur CMOS à haut-débit," *Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications*, pp. 119-122, Louvain-la-Neuve, Belgium, 25-26 Sept. 2003
15. M. Brière, F. Mieyeville, I. O'Connor, F. Gaffiot, "Un réseau d'interconnexion optique passif basé sur le routage en longueur d'onde," *Symposium en Architecture et Adéquation Algorithme Architecture*, pp. 425-432, La Colle-sur-Loup, France, 15-17 Oct. 2003
16. I. O'Connor, F. Mieyeville, F. Tissafi-Drissi, G. Tosik, F. Gaffiot, "Predictive Design Space Exploration of Maximum Bandwidth CMOS Photoreceiver Preamplifiers," *IEEE International Conference on Electronics, Circuits and Systems*, pp. 483-486, Sharjah, United Arab Emirates, 14-17 December 2003
17. F. Tissafi-Drissi, I. O'Connor, F. Gaffiot, "RUNE: Platform for automated design of integrated multi-domain systems. Application to high-speed CMOS photoreceiver front-ends," *Design Automation and Test in Europe*, pp. 16-21, Paris, France, 16-20 February 2004
18. G. Tosik, Z. Lisik, M. Langer, F. Gaffiot, I. O'Connor, "Simulation of Electrical and Optical Interconnections for Future VLSI ICs," *International Conference on Computational Science*, pp.1037-1044, Krakow, Poland, 6-9 June 2004
19. M. Brière, L. Carrel, T. Michalke, F. Mieyeville, I. O'Connor, F. Gaffiot, "Design and behavioral modeling tools for optical networks on chip," *Design Automation and Test in Europe*, pp. 738-739, Paris, France, 16-20 February 2004
20. E. Drouard, M. Brière, F. Mieyeville, I. O'Connor, X. Letartre and F. Gaffiot, "Optical Network On-chip Multi-Domain modeling using SystemC," *Proc. Forum on Specification and Design Languages*, pp. 123--134, Lille, France, 14-17 September 2004
21. M. Brière, E. Drouard, F. Tissafi-Drissi, F. Mieyeville, I. O'Connor and F. Gaffiot, "SystemC modeling of an Optical Network-on-Chip using VCI protocol," *Proc. GSPx*, Santa Clara, CA, USA, September 2004
22. E. Drouard, M. Brière, A. Kazmierczak, X. Letartre, I. O'Connor, F. Gaffiot, "Phenomenological modeling of WDM crossbars based on channel drop filters," *13th International Workshop on Optical Waveguide Theory and Numerical Modeling (OWTNM 2005)*, 8 – 9 April 2005, Grenoble
23. A. Kazmierczak, M. Brière, E. Drouard, P. Rojo-Romeo, I. O'Connor, X. Letartre, F. Gaffiot, L. El Melhaoui, P. Lyan, J.M. Fedeli, "Design and characterization of optical networks on chip," *12th European Conference on Integrated optics (ECIO 2005)*, 6 – 8 April 2005, Grenoble
24. M. Brière, E. Drouard, F. Mieyeville, D. Navarro, I. O'Connor, F. Gaffiot, "Heterogeneous modeling of an optical network on chip with SystemC," *Proc. IEEE International Workshop on Rapid System Prototyping*, pp. 10-16, Montreal, Canada, 8-10 June 2005
25. M. Owczarek, I. O'Connor, "Program RUNE as an Example of Usage of Computers in Optimization Processes," *International Conference Microtherm*, Lodz (Poland), 19-22 June 2005
26. I. O'Connor, F. Tissafi-Drissi, G. Revy, F. Gaffiot, "UML/XML-based approach to hierarchical AMS synthesis," *Proc. Forum on Design Languages*, pp. 89-100, Lausanne, Switzerland, September 27-30 2005

27. D. Navarro, D. Ramat, F. Mieyeville, I. O'Connor, F. Gaffiot, "VHDL & VHDL-AMS modeling and simulation of a CMOS imager IP," *Proc. Forum on Design Languages*, pp. 179-182, Lausanne, Switzerland, September 27-30 2005
28. D. Navarro, M. Brière, I. O'Connor, F. Mieyeville, F. Gaffiot, L. Carrel, "Quantitative study of area and power consumption costs for 3 Gbits/s optical communications in a 0.13µm CMOS circuit," *20th Conference on Design of Circuits and Integrated Systems*, Lisbon, Portugal, 23–25 November 2005
29. B. Payet, P. Vincent, I. O'Connor, F. Gaffiot, "A fully-integrated 60 GHz VCO in l3Onm SOI-CMOS on high-resistivity substrate," *Ph. D. Research in Microelectronics and Electronics (PRIME)*, pp. 105-108, Otranto (Lecce), Italy, 12-15 June 2006
30. S. Dia, F. Mieyeville, I. O'Connor, F. Gaffiot, "Modeling and simulation of radiofrequency circuit blocks for performance evaluation in a system-on-chip context," *Int. Symp. Performance Evaluation of Computer and Telecommunication Systems*, Calgary, Canada, July 31-August 2, 2006
31. S. Dia, F. Mieyeville, I. O'Connor, F. Gaffiot, "Radio-frequency link modeling and simulation in a system-on-chip context," *European Modeling Symposium*, London, United Kingdom, 11-12 September 2006
32. M. Owczarek, G. Tosik, Z. Lisik, I. O'Connor, "Optimization of the On-Chip Optical Receivers," *IXth International Conference CADSM*, pp. 130-133, Polyana (Ukraine), 20-24 February 2007
33. M. Brière, B. Girodias, Y. Bouchebaba, G. Nicolescu, F. Mieyeville, F. Gaffiot, I. O'Connor, "System Level Assessment of an Optical NoC in an MPSoC Platform," *Design Automation and Test in Europe (DATE)*, Nice, France, 16-20 April 2007
34. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Design of a Novel CNTFET-based Reconfigurable Logic Gate," *IEEE Symp. VLSI*, Porto Alegre, Brazil, 9-11 May 2007
35. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Novel CNTFET-based Reconfigurable Logic Gate Design," *Design Automation Conference (DAC)*, San Diego, CA, USA, 4-8 June 2007
36. M. Brière, L. Gheorghe, G. Nicolescu, I. O'Connor, "Formalization of Optical Networks on Chip using DEVS Formalism," *Summer Computer Simulation Conference*, 14-19 July 2007, San Diego, CA, USA
37. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Design of a Family of Novel CNTFET-based Dynamically Reconfigurable Logic Gates," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 698-701
38. I. Hassoune, I. O'Connor, D. Navarro, "On the performance of Double-Gate MOSFET circuit applications," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 558-561
39. M. Brière, B. Girodias, Y. Bouchebaba, G. Nicolescu, F. Mieyeville, F. Gaffiot, I. O'Connor, "Architectural Exploration of Optical and Electrical Interconnects in MPSoC," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 1469-1472
40. M. Brière, L. Gheorghe, G. Nicolescu, I. O'Connor, "Towards the High-Level Design of Optical Networks-on-Chip: Formalization of Opto-Electrical Interfaces," *IEEE International Conference on Electronics, Circuits and Systems*, 11-14 December 2007, Marrakech, Morocco
41. I. Hassoune, X. Yang, I. O'Connor, D. Navarro, "Using SOI Double-Gate MOSFET NDR Structures to Improve Ultra-Low Power Full Adder Performance," *IEEE-NEWCAS/TAISA Conference*, June 22-25, 2008, Montreal, Canada
42. I. Hassoune, I. O'Connor, D. Navarro, "Design of a Family of Gate-level Reconfigurable Logic Cells Based on Double-Gate MOSFETs," *16th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 13-15 2008, Rhodes Island, Greece
43. J. Liu, I. O'Connor, D. Navarro and F. Gaffiot, "Dynamically reconfigurable CNTFET logic cell matrix programming methods," *16th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 13-15 2008, Rhodes Island, Greece
44. I. O'Connor, F. Mieyeville, F. Gaffiot, A. Scandurra, G. Nicolescu, "Reduction methods for adapting optical network on chip topologies to specific routing applications," *Design of Circuits and Integrated Systems (DCIS)*, November 12-14 2008, Grenoble, France
45. A. Scandurra, I. O'Connor, "Scalable CMOS-compatible photonic routing topologies for versatile networks on chip," *International Workshop on Network on Chip Architectures (NocArc)*, November 8th 2008, Lake Como, Italy
46. H. Filiol, I. O'Connor, D. Morche, "A new approach for variability analysis of analog ICs," *IEEE-NEWCAS/TAISA Conference*, June 29 – July 1, 2009, Toulouse, France

47. P.E. Gaillardon, I. O'Connor, J. Liu, R. Daviot, N. Abouchi, F. Clermidy, "Interconnection scheme and associated mapping method of reconfigurable cell matrices based on nanoscale devices," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, July 30-31 2009, San Francisco (CA), USA
48. H. Filiol, I. O'Connor, D. Morche, "Piecewise-Polynomial Modeling for Analog Circuit Performances", *European Conference on Circuit Theory & Design (ECCTD'09)*, 23-27 August 2009, Antalya, Turkey
49. L. Gheorghe Iugan, G. Nicolescu, I. O'Connor, "Modeling and Formal Verification of a Passive Optical Network on Chip Behavior," *Proc. 3rd International Workshop on Multi-Paradigm Modeling (MPM 2009)*, 6 October 2009, Denver (CO), USA
50. P.E. Gaillardon, I. O'Connor, J. Liu, R. Daviot, N. Abouchi, F. Clermidy, "Mapping Method of Reconfigurable Cell Matrices Based on Nanoscale Devices Using Inter-Stage Fixed Interconnection Scheme," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 13-16 December 2009, Hammamet, Tunisia
51. P.E. Gaillardon, F. Clermidy, I. O'Connor, R. Daviot, "Reconfigurable logic cells for nanoscale – Comparison between density and functionality enhancement," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 13-16 December 2009, Hammamet, Tunisia
52. A. Allam, I. O'Connor, "Optical NOC Design-Parameters Exploration and Analysis," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 13-16 December 2009, Hammamet, Tunisia
53. O. Valorge, F. Calmon, M. Le Berre, C. Gontrand, E. Eid, T. Lacrevaz, F. Flechet, J. Charbonnier, I. O'Connor, CEM 2010 "Modélisation RLCG de lignes coplanaires sur un substrat silicium avec couche épitaxiée pour applications CMOS", *Colloque International sur la Compatibilité Electromagnétique*, 7-9 April 2010, Limoges, France
54. H. Filiol, I. O'Connor, D. Morche, "Variability Analysis of ICs using the Cornish-Fisher Approximation," *European Workshop on CMOS Variability (VARI)*, May 26-27 2010, Montpellier, France
55. A. Allam, I. O'Connor, W. Heirman, "Performance Evaluation for Passive-Type Optical Network-on-Chip," *IEEE International Symposium on Rapid System Prototyping (RSP)*, June 8-11 2010, Fairfax (VA), USA
56. K. Jabeur, D. Navarro, I. O'Connor, P.E. Gaillardon, M.H. Ben Jamaa, F. Clermidy, "Reducing transistor count in clocked standard cells with ambipolar double-gate FETs," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, July 17-18 2010, Anaheim (CA), USA
57. B. Wang, L. Labrak, I. O'Connor, E. Drouard, "Bottom-up Verification Methodology for CMOS Photonic Linear Heterogeneous System," *Forum on specification & Design Languages (FDL 2010)*, September 14-16 2010, Southampton, UK
58. F. Yengui, L. Labrak, F. Frantz, I. O'Connor, T. Tixier, N. Abouchi, "Comparison of hybrids PSO-SQP and GA-SQP For Transimpedance Amplifier and Optical Driver," *Int. Conf. Metaheuristics and Nature Inspired Computing (META'10)*, October 27-30 2010, Djerba, Tunisia
59. P.E. Gaillardon, M.H. Ben-Jamaa, M. Reyboz, G.B. Beneventi, F. Clermidy, L. Perniola, I. O'Connor, "Phase-Change-Memory-Based Storage Elements for Configurable Logic," *Int. Conf. Field-Programmable Technology (FPT'10)*, December 8-10 2010, Beijing, China
60. B. Wang, I. O'Connor, E. Drouard, "Passive Component Modeling for Optical Network-on-Chip," *Asia Communications & Photonics Conference & Exhibition (ACP 2010)*, December 8-12 2010, Shanghai, China
61. I. O'Connor, K. Jabeur, D. Navarro, N. Yakymets, P.E. Gaillardon, M.H. Ben-Jamaa, F. Clermidy, "Logic cells and interconnect strategies for nanoscale reconfigurable computing fabrics," *IEEE Int. Conf. Electronics, Circuits, and Systems (ICECS)*, 12-15 December 2010, Athens, Greece
62. M. H. Ben Jamaa, P. E. Gaillardon, S. Frégonèse, M. De Marchi, G. De Micheli, T. Zimmer, I. O'Connor, F. Clermidy, "FPGA Design with Double-Gate Carbon Nanotube Transistors," *China Semiconductor Technology International Conference (CSTIC)*, 13-14 March 2011, Shanghai, China
63. S. Le Beux, J. Trajkovic, G. Nicolescu, G. Bois, P. Paulin, I. O'Connor, "Optical ring network-on-chip (ORNOC) architecture and design methodology," *Design Automation and Test in Europe (DATE) 2011*, 14-18 March 2011, Grenoble, France
64. A. Fourmigue, G. Beltrame, G. Nicolescu, E.M. Aboulhamid, I. O'Connor, "Multi-granularity thermal evaluation of 3D MPSOC architectures," *Design Automation and Test in Europe (DATE) 2011*, 14-18 March 2011, Grenoble, France
65. K. Jabeur, N. Yakymets, I. O'Connor, S. Le Beux, "Fine-Grain Reconfigurable Logic Cells Based on Double-gate CNTFETs," *IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI) 2011*, 2-4 May 2011, Lausanne, Switzerland
66. P.E. Gaillardon, M. H. Ben-Jamaa, F. Clermidy, I. O'Connor, "Evaluation of a Crossbar Multiplexer in a Lithography-Based Nanowire Technology," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 15-18 May 2011, Rio de Janeiro, Brazil

67. N. Yakymets, K. Jabeur, I. O'Connor, S. Le Beux, "Interconnect Topology for Cell Matrices Based on Low-Power Nanoscale Devices," *Faible Tension Faible Consommation (FTFC)*, 30 May – 1 June 2011, Marrakech, Morocco
68. P.E. Gaillardon, M. H. Ben-Jamaa, F. Clermidy, I. O'Connor, "Can we go towards true 3D architectures?" ACM Design Automation Conference *(DAC)*, San Diego (CA), USA, 6-10 June 2011
69. P.E. Gaillardon, M. H. Ben-Jamaa, F. Clermidy, I. O'Connor, "Ultra-Fine Grain FPGAs: A Granularity Study", *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, San Diego (CA), USA, 8-9 June 2011
70. K. Jabeur, N. Yakymets, I. O'Connor, S. Le Beux, "Ambipolar double-gate FET binary-decision diagram (Am-BDD) for reconfigurable logic cells," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, San Diego (CA), USA, 8-9 June 2011
71. D. Navarro, F. Mieyeville, W. Du, M. Galos, I. O'Connor, "Towards a Design Framework for Heterogeneous Wireless Sensor Networks," *International Symposium on Access Spaces (IEEE-ISAS)*, Yokohama, Japan, 17-19 June 2011
72. N. Yakymets, K. Jabeur, I. O'Connor, S. Le Beux, "Mapping Methodology and Analysis of Matrix-Based Nanocomputer Architectures," *9th IEEE International NEWCAS Conference*, Bordeaux, France, 26-29 June 2011 **(Recipient of Best Paper Award)**
73. V. Viswanathan, L. Labrak, F. Frantz, D. Navarro and I. O'Connor, "Model based design of imager using abstraction-segregated parameter dependency graphs," *9th IEEE International NEWCAS Conference*, Bordeaux, France, 26-29 June 2011
74. M. Galos, D. Navarro, F. Mieyeville, I. O'Connor, "Energy-Aware Software Updates in Heterogeneous Wireless Sensor Networks," *9th IEEE International NEWCAS Conference*, Bordeaux, France, 26-29 June 2011
75. F. Frantz, L. Labrak, I. O'Connor, "3D-IC Floorplanning: Applying Meta-Optimization to Improve Performance," *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Hong Kong, China, 3-5 October 2011
76. M. Galos, D. Navarro, F. Mieyeville, I. O'Connor, "Reprogramming hardware-software heterogeneous Wireless Sensor Networks," *14th International Symposium on Wireless Personal Multimedia Communications (WPMC)*, Brest, France, 3-6 October 2011
77. W. Du, D. Navarro, F. Mieyeville, I. O'Connor, "IDEA1: A Validated System-level Simulator for Wireless Sensor Networks," *4th International Workshop on Wireless Sensor, Actuator and Robot Networks (WiSARN-FALL 2011)*, Valencia, Spain, 17-22 October 2011
78. H. Zhu, S. Le Beux, I. O'Connor, "Using Self-Reconfiguration to Increase Manufacturing Yield of CNTFET-Based Architectures;" *International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, Cancun, Mexico, 30 November – 2 December 2011
79. D. Navarro, Z. Feng, V. Viswanathan, L. Carrel, I. O'Connor, "Image toolbox for CMOS image sensors simulations in Cadence ADE," *International Conference on Design and Modeling in Science, Education, and Technology (DeMset)*, Orlando (FL), USA, 29 November – 2 December 2011
80. K. Jabeur, I. O'Connor, N. Yakymets, S. Le Beux, "High Performance 4:1 Multiplexer with Ambipolar Double-Gate FETs," *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Beirut, Lebanon, 11-14 December 2011
81. A. Allam, I. O'Connor, "A Protocol Stack Architecture for Optical Network-on-Chip," *International Conference on Computing and Information Technology*, Al-Madinah Al-Munawwarah, Saudi Arabia, 12-14 March 2012
82. K. Jabeur, I. O'Connor, N. Yakymets, S. Le Beux, "Ambipolar double-gate FETs for the design of compact logic structures," *IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI) 2012*, Salt Lake City (UT), USA, 3-4 May 2012
83. M. Galos, D. Navarro, F. Mieyeville, I. O'Connor, "A cycle-accurate transaction-level modeled energy simulation approach for heterogeneous Wireless Sensor Networks," *IEEE 10th International New Circuits and Systems Conference (NEWCAS)*, pp. 209–212, Montreal, Canada, 17-20 June 2012
84. K. Jabeur, I. O'Connor, D. Navarro, S. Le Beux, "Low-power design technique with ambipolar double gate devices," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, Amsterdam, Netherlands, 4-6 July 2012
85. K. Jabeur, I. O'Connor, S. Le Beux, D. Navarro, "Ambipolar double gate CNTFET based reconfigurable logic cells," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, Amsterdam, Netherlands, 4-6 July 2012
86. Z. Feng, V. Viswanathan, D. Navarro, I. O'Connor, "Image sensor matrix high speed simulation," *WASET International Conference on Electronics, Circuits, and Systems (ICECS)*, Venice, Italy, 14-16 November 2012

87. N. Zhu, I. O'Connor, "Energy Performance of High Data Rate and Low Power Transceiver based Wireless Body Area Networks," Int. Conf. Sensor Networks (Sensornets), pp. 141-144, Barcelona, Spain, 19-22 February 2013
88. Z. Li, S. Le Beux, C. Monat, X. Letartre, I. O'Connor, "Optical Look Up Table," *Design Automation and Test in Europe (DATE) 2013*, Grenoble, France, 18-22 March 2013 (DOI: 10.7873/DATE.2013.184)
89. N. Zhu, I. O'Connor, "Energy Measurements and Evaluations on High Data Rate and Ultra Low Power WSN Node," *IEEE International Conference on Networking Sensing and Control (ICNSC)*, pp. 232-236, Paris, France, 10-12 April 2013 (DOI: 10.1109/ICNSC.2013.6548742)
90. P. Coudrain, D. Henry, A. Berthelot, J. Charbonnier, S. Verrun, R. Franiatte, N. Bouzaida, G. Cibrario, F. Calmon, I. O'Connor, T. Lacrevaz, L. Fourneaud, B. Flechet, N. Chevrier, A. Farcy, O. Le-Briz, "3D Integration of CMOS image sensor with coprocessor using TSV last and micro-bumps technologies," *IEEE Electronic Components and Technology Conference (ECTC)*, pp. 674-382, Las Vegas (NV), USA, 28-31 May 2013 (DOI: 10.1109/ECTC.2013.6575646)
91. N. Zhu, I. O'Connor, "Performance evaluations of unslotted CSMA/CA algorithm at high data rate WSNs scenario," *9th IEEE International Wireless Communications and Mobile Computing Conference (IWCMC)*, pp. 406-411, Cagliari, Italy, 1-5 July 2013 (DOI: 10.1109/IWCMC.2013.6583593)
92. K. Cheng, S. Le Beux, I. O'Connor, "Am/IDG-FET based Reconfigurable Cells versus LUTs: Characteristics Description and Analysis," *25th IEEE Int. Conf. Microelectronics (ICM)*, Beirut, Lebanon, pp. 1-4, 15-18 December 2013 (DOI: 10.1109/ICM.2013.6734987)
93. R. Cao, L. Couder, J. Cayo, J. Ferguson, F. Pikus, A. Arriordaz, I. O'Connor, "Curvilinear Property Measurement and Computation Methods for Physical Verification of Bent Waveguides in Photonic Integrated Circuit Layouts," *IEEE Optical Interconnects Conference*, San Diego, 20-22 April 2014 (DOI: 10.1109/OIC.2014.6886066)
94. S. Le Beux, F. Alibart, D. Vuillaume, C. Dubourdieu, I. O'Connor, "Memristive devices: an interconnect solution for matrix-based architectures?" *Symposium S: Memristor materials, mechanisms and devices for unconventional computing*, *E-MRS 2014 Spring Meeting*, Lille, France, 26-30 May 2014
95. R. Cao, J. Ferguson, Y. Drissi, F. Gays, A. Arriordaz, I. O'Connor, "DRC Challenges and Solutions for Non-Manhattan Layout Designs," *International Conference on Optical MEMS and Nanophotonics (OMN)*, Glasgow, UK, 17-21 August 2014 (DOI: 10.1109/OMN.2014.6924580)
96. R. Cao, H. Hu, J. Ferguson, F. Pikus, J. Cayo, A. Arriordaz, E. Cassan, W. Bogaerts, I. O'Connor, "Photonics Design with an EDA approach: Validation of Layout Waveguide Interconnects," *IEEE 11th International Conference on Group IV Photonics (GFP)*, Paris, France, 27-29 August 2014 (DOI: 10.1109/Group4.2014.6961992)
97. R. Cao, J. Ferguson, F. Gays, Y. Drissi, A. Arriordaz, I. O'Connor, "Silicon Photonics Design Rule Checking: Application of a Programmable Modeling Engine for Non-Manhattan Geometry Verification," *IEEE/IFIP 22nd International Conference on VLSI and System-on-Chip (VLSI-SoC)*, Playa del Carmen, Mexico, 6-8 October 2014 (DOI: 10.1109/VLSI-SoC.2014.7004173)
98. Z. Li, S. Le Beux, C. Monat, I. O'Connor, X. Letartre, "Complementary logic interface for high performance optical computing with OLUT," *IEEE/IFIP 22nd International Conference on VLSI and System-on-Chip (VLSI-SoC)*, Playa del Carmen, Mexico, 6-8 October 2014 (DOI: 10.1109/VLSI-SoC.2014.7004178)
99. J. Luo, C. Killian, S. Le Beux, D. Chillet, H. Li, I. O'Connor, O. Sentieys, "Channel Allocation protocol for reconfigurable Optical Network-on-Chip," Workshop on Exploiting Silicon Photonics for Energy-Efficient High-Performance Computing (SiPhotonics), Amsterdam, The Netherlands, 19-21 January 2015 (DOI: 10.1109/SiPhotonics.2015.12)
100. H. Li, S. Le Beux, I. O'Connor, G. Nicolescu, "Energy-Efficient Optical Crossbars on Chip with Multi-Layer Deposited Silicon," *20th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 148-153, Tokyo, Japan, 19-22 January 2015 (DOI: 10.1109/ASPDAC.2015.7058996)
101. H. Li, A. Fourmigue, S. Le Beux, X. Letartre, I. O'Connor, G. Nicolescu, "Thermal-Aware Design Method for On-Chip Optical Interconnect," *Design Automation and Test in Europe (DATE) 2015*, Grenoble, France, 9-13 March 2015
102. R. Cao, J. Billoudet, J. Ferguson, L. Couder, J. Cayo, A. Arriordaz, I. O'Connor, "LVS Check for Photonic Integrated Circuit – Curvilinear Feature Extraction and Validation," *Design Automation and Test in Europe (DATE) 2015*, Grenoble, France, 9-13 March 2015
103. F. Teysseyre, D. Navarro, I. O'Connor, F. Cascio, F. Cenni, O. Guillaume, "Fast optical simulation from a reduced set of impulse responses using SystemC AMS," *Design Automation and Test in Europe (DATE)*, pp. 405-409, Grenoble, France, 9-13 March 2015 (DOI: 10.7873/DATE.2015.0284)

104. H. Li, S. Le Beux, Y. Thonnart, I. O'Connor, "Complementary Communication Path for Energy Efficient on-chip Optical Interconnects," *ACM Design Automation Conference (DAC)*, San Francisco (CA), USA, 7-11 June 2015 (DOI= 10.1145/2744769.2744810)
105. Q. An, L. Su, J. O. Klein, S. Le Beux, I. O'Connor, W. Zhao, "Full-adder circuit design based on all-spin logic device," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 163-168, Boston (MA), USA, 8-10 July 2015 (DOI: 10.1109/NANOARCH.2015.7180606)
106. R. Cao, J. Ferguson, A. Bakker, T. Korthorst, A. Arriordaz, I. O'Connor, "Photonic designs with EDA approach: A novel methodology for curve design validation," *IEEE Photonics Summer Topicals Meeting Series (SUM)*, pp. 29-30, Nassau, Bahamas, 13-15 July 2015 (DOI: 10.1109/PHOSST.2015.7248177)
107. J. Sepulveda, S. Le Beux, J. Luo, C. Killian, D. Chillet, H. Li, I. O Connor, O. Sentieys, "Communication Aware Design Method for Optical Network-on-Chip," *IEEE 9th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, pp. 243-250, Turin, Italy, 23-25 September 2015 (DOI: 10.1109/MCSoC.2015.33)
108. H. Li, A. Fourmigue, S. Le Beux, I. O'Connor, G. Nicolescu, "A Thermal-Aware Laser Tuning Approach for Silicon Photonic Interconnects," *2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)*, Dresden, Germany, 18 March 2016
109. O. Sentieys, J. Sepulveda, S. Le Beux, J. Luo, C. Killian, D. Chillet, I. O'Connor, H. Li, "Design Space Exploration of Optical Interfaces for Silicon Photonic Interconnects," *2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)*, Dresden, Germany, 18 March 2016
110. R. Cao, J. Ferguson, C. Cone, A. Arriordaz, I. O'Connor, "Enabling Silicon Photonics Technology with EDA," *2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)*, Dresden, Germany, 18 March 2016
111. J. Luo, C. Killian, D. Chillet, S. Le Beux, I. O'Connor, O. Sentieys, "Wavelength Allocation for Efficient Communications on Optical Network-on-Chip," *ECSI Conference on Design and Architectures for Signal and Image Processing (DASIP)*, pp.1656-1658, Rennes, France, 12-14 October 2016
112. C. Killian, D. Chillet, S. Le Beux, O. Sentieys, V.D. Pham, I. O'Connor, "Energy and Performance Trade-off in Nanophotonic Interconnects using Coding Techniques," *IEEE/ACM Design Automation Conference (DAC)*, Austin (TX), USA, 18-22 June 2017 (DOI: 10.1145/3061639.3062237)
113. Q. An, S. Le Beux, I. O'Connor, J.O. Klein, W. Zhao, "Arithmetic Logic Unit based on all-spin logic devices," *IEEE International New Circuits and Systems Conference (NEWCAS)*, pp. 317-320, Strasbourg, France, 25-28 June 2017 (DOI: 10.1109/NEWCAS.2017.8010169)
114. A. Perodou, A. Korniienko, M. Zarudniev, G. Scorletti, I. O'Connor, J.B. David, "On Motivations for Designing Analog Filters Under LFT Framework," *20th World Congress of the International Federation of Automatic Control (IFAC)*, Toulouse, France, 9-14 July 2017
115. K. Cheng, S. Le Beux, I. O'Connor, "Hybrid Topologies for Reconfigurable Matrices Based on Nano-Grain Cells," *IEEE International Conference on Rebooting Computing (ICRC)*, Washington (DC), USA, 8th-9th November 2017 (DOI: 10.1109/ICRC.2017.8123639)
116. Z. Li, C. Monat, S. Le Beux, X. Letartre, I. O'Connor, "An Energy-Efficient Reconfigurable Nanophotonic Computing Architecture Design: Optical Lookup Table," *IEEE International Conference on Rebooting Computing (ICRC)*, Washington (DC), USA, 8th-9th November 2017 (DOI: 10.1109/ICRC.2017.8123670)
117. Q. An, S. Le Beux, I. O'Connor, J.O. Klein, "Large scale, high density integration of all spin logic," *Design, Automation and Test in Europe (DATE)*, Dresden, Germany, 19-23 March 2018 (DOI: 10.23919/DATE.2018.8341992)
118. A. Perodou, A. Korniienko, G. Scorletti, I. O'Connor, "Design Method of Passive Ladder Filters using a Generalized Variable: a First Step," *IEEE Conference on Design of Circuits and Integrated Systems*, Lyon, France, 14-16 November 2018 (DOI: 10.1109/DCIS.2018.8681463)
119. S. Rigault, N. Moeneclaey, L. Labrak, Ian O'Connor, "CMOS VCSEL driver dedicated for sub-nanosecond laser pulses generation in SPAD-based time-of-flight rangefinder", *IEEE Conference on Design of Circuits and Integrated Systems*, Lyon, France, 14-16 November 2018 (DOI: 10.1109/DCIS.2018.8681460)
120. S. Rigault, N. Moeneclaey, L. Labrak, Ian O'Connor, "A Low-Voltage Sub-ns Pulse Integrated CMOS Laser Diode Driver for SPAD-based Time-of-Flight Rangefinding in Mobile Applications", *IEEE International System-on-Chip Conference (SOCC)*, Singapore, 3-6 September 2019 (DOI: 10.1109/SOCC46988.2019.1570548090)

121. A. Brik, L. Labrak, L. Carrel, I. O'Connor, R. Iskander, "Fast extraction of predictive models for integrated circuits using n-performances Pareto fronts", *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)*, Cuzco, Peru, 6-9 October 2019 (DOI: 10.1109/VLSI-SoC.2019.8920305)
122. E. Dupuis, D. Novo, I. O'Connor, A. Bosio, "On the Automatic Exploration of Weight Sharing for Deep Neural Network Compression", *Design, Automation and Test in Europe (DATE)*, Grenoble, France, 9-13 March 2020 (DOI: 10.23919/DATE48585.2020.9116350)
123. A. Bosio, I. O'Connor, G.S. Rodrigues, F.K. Lima, S. Hamdioui, "Exploiting Approximate Computing for implementing Low Cost Fault Tolerance Mechanisms," *Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Marrakech, Morocco, 1-3 April 2020 (DOI: 10.1109/DTIS48698.2020.9081268)
124. E. Dupuis, D. Novo, I. O'Connor, A. Bosio, "Sensitivity Analysis and Compression Opportunities in DNNs Using Weight Sharing," *Int. Symp. Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, Novi Sad, Serbia, 22-24 April 2020 (DOI: 10.1109/DDECS50862.2020.9095658)
125. A. Brik, L. Labrak, I. O'Connor, D. Saias, "Fast hierarchical system synthesis based on predictive models," *IEEE International New Circuits and Systems Conference (NEWCAS)*, Montreal (QC), Canada, 16-19 June 2020 (DOI: 10.1109/NEWCAS49341.2020.9159765)
126. A. Poittevin, C. Mukherjee, I. O'Connor, C. Maneux, G. Larrieu, A. Kumar, F. Marc, A. Lecestre, M. Deng, S. Le Beux, "3D logic cells design and results based on Vertical NWFET technology including tied compact model," IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC), Salt Lake City (UT), USA [virtual], 5-9 October 2020 (DOI: 10.1109/VLSI-SOC46417.2020.9344094)
127. E. Dupuis, D. Novo, I. O'Connor, A. Bosio, "Fast exploration of weight sharing opportunities for CNN compression" DATE 2021 Friday Workshop on System-level Design Methods for Deep Learning on Heterogeneous Architectures (SLOHA 2021), Grenoble (virtual), France, 5th February 2021
128. O. Sentieys, S. Filip, D. Briand, D. Novo, E. Dupuis, I. O'Connor, A. Bosio, "AdequateDL: Approximating Deep Learning Accelerators," *International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, p. 37-40, Vienna, Austria, 7-9 April 2021 (DOI: 10.1109/DDECS52668.2021.9417026)
129. A. Bosio, I. O'Connor, M. Traiola, J. Echavarria, J. Teich, M.A. Hanif, M. Shafique, S. Hamdioui, B. Deveautour, P. Girard, A. Virazel, K. Bertels, "Emerging Computing Devices: Challenges and Opportunities for Test and Reliability," 26th IEEE European Test Symposium (ETS), virtual, 24-28 May 2021 (DOI: 10.1109/ETS50041.2021.9465409)
130. F. Pavanello, I. O'Connor, U. Rührmair, A.C. Foster, D. Syvridis, "Recent Advances in Photonic Physical Unclonable Functions," 26th IEEE European Test Symposium (ETS), virtual, 24-28 May 2021 (DOI: 10.1109/ETS50041.2021.9465434)
131. C. Zrounba, S. Cueff, S. Le Beux, I. O'Connor, F. Pavanello, "Exploration of the optical behavior of phase-change materials integrated in silicon photonics platforms," Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC), virtual, 21-25 June 2021 (DOI: 10.1109/CLEO/Europe-EQEC52157.2021.9542745)
132. C. Marchand, I. O'Connor, M. Cantan, E.T. Breyer, S. Slesazeck, T. Mikolajick, "FeFET based Logic-in-Memory: an overview," 16th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS), Apulia, Italy, 28-30 June 2021, (DOI: 10.1109/DTIS53253.2021.9505078)
133. I. O'Connor, A. Poittevin, S. Le Beux, A. Bosio, Z. Stanojevic, O. Baumgartner, C. Mukherjee, C. Maneux, J. Trommer, T. Mikolajick, G. Larrieu, "Analysis of Energy-Delay-Product of a 3D Vertical Nanowire FET Technology," 2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS), Caen, France, 1-3 September 2021, (DOI: 10.1109/EuroSOI-ULIS53016.2021.9560180)
134. M. Traiola, J. Echavarria, A. Bosio, J. Teich, I. O'Connor, "Design Space Exploration of Approximation-Based Quadruple Modular Redundancy Circuits," IEEE/ACM International Conference On Computer-Aided Design (ICCAD), Munich (virtual), Germany, 1-5 November 2021 (DOI: 10.1109/ICCAD51958.2021.9643561)
135. C. Maneux, C. Mukherjee, M. Deng, M. Dubourg, L. Reveil, G. Bordea, A. Lecestre, G. Larrieu, J. Trommer, E.T. Breyer, S. Slesazeck, T. Mikolajick, O. Baumgartner, M. Karner, D. Pirker, Z. Stanojevic, David A. Atienza, A. Levisse, G. Ansaloni, A. Poittevin, A. Bosio, D. Deleruyelle, C. Marchand, I. O'Connor, "Modelling of vertical and ferroelectric junctionless technology for efficient 3D neural network compute cube dedicated to embedded artificial intelligence," *IEEE International Electron Device Meeting (IEDM), San Francisco (CA)*, USA, 11-15 December 2021 (DOI: 10.1109/IEDM19574.2021.9720572)

136. E. Dupuis, D. Novo, I. O'Connor, A. Bosio, "A Heuristic Exploration to Retraining-free Weight Sharing for CNN Compression," *ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 134 – 139, Taipei, Taiwan (virtual), 17-20 January 2022 (DOI: 10.1109/ASP-DAC52403.2022.9712487)
137. C. Bolchini, A. Bosio, L. Cassano, B. Deveautour, G. Di Natale, A. Miele, I. O'Connor, I. Vatajelu, "Dependability of Alternative Computing Paradigms for Machine Learning: hype or hope?" *IEEE Int. Symp. Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, Prague, Czech Republic, 6-8 April 2022 (DOI: 10.1109/DDECS54261.2022.9770138)
138. M. Barbareschi, A. Bosio, I. O'Connor, P. Fišer, M. Traiola, "A Design Space Exploration Framework for Memristor-Based Crossbar Architecture," *IEEE Int. Symp. Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, Prague, Czech Republic, 6-8 April 2022 (DOI: 10.1109/DDECS54261.2022.9770145)
139. M. Abdalla, C. Zrounba, R. Cardoso, G. Ren, A. Boes, A. Mitchell, A. Bosio, I. O'Connor, F. Pavanello, "Photonic time-delay reservoir computing based on an asymmetric Mach-Zehnder interferometer with reconfigurable memory capacity," *23rd European Conference on Integrated Optics (ECIO)*, Milan, Italy, 4-6 May 2022 (https://hal.science/hal-03754438)
140. A. Piri, S. Sepide, M. Barbareschi, B. Deveautour, S. Di Carlo, I. O'Connor, A. Savino, M. Traiola, A. Bosio, "Input-Aware Approximate Computing," *IEEE International Conference on Automation, Quality and Testing, Robotics (AQTR)*, Cluj-Napoca, Romania, 19-21 May, 2022 (DOI: 10.1109/AQTR55203.2022.9801944)
141. A. Poittevin, C. Marchand, A. Bosio, I. O'Connor, C. Maneux, C. Mukherjee, "A Logic Cell and routing Methodology Specific to VNWFET," *IEEE Int. New Circuits and Systems Conference (NEWCAS), Quebec City (QC)*, Canada, 19-22 June 2022 (DOI: 10.1109/NEWCAS52662.2022.9842100)
142. R. Cardoso, L. Arif, C. Zrounba, F. Pavanello, I. O'Connor, L. Virot, S. Le Beux, "Energy Efficient on-Chip Optical Broadcast with partial-Absorption Photodiodes," *IEEE Int. New Circuits and Systems Conference (NEWCAS)*, Quebec City (QC), Canada, 19-22 June 2022 (DOI: 10.1109/NEWCAS52662.2022.9842233)
143. P.A. Matrangolo, C. Marchand, I. O'Connor, D. Navarro, "Hardware Emulation of FeFET on FPGA," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pafos, Cyprus, 4-6 July 2022 (DOI: 10.1109/ISVLSI54635.2022.00085)
144. A. Bosio, B. Deveautour, I. O'Connor, "Exploiting Approximate Computing for Efficient and Reliable Convolutional Neural Networks," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pafos, Cyprus, 4-6 July 2022 (DOI: 10.1109/ISVLSI54635.2022.00070)
145. C. Maneux, C. Mukherjee, M. Deng, B. Neckel Wesling, L. Réveil, Z. Stanojevic, O. Baumgartner, I. O'Connor, A. Poittevin, G. Larrieu, "Circuit Design Flow dedicated to 3D vertical nanowire FET," *IEEE Latin American Electron Devices Conference (LAEDC)*, Puebla, Mexico, 4-6 July 2022 (DOI: 10.1109/LAEDC54796.2022.9908233)
146. C. Zrounba, R. Cardoso, M. Abdalla, S. Cueff, A. Bosio, S. Le Beux, X. Letartre, I. O'Connor, F. Pavanello, "Comparing Rib and Slot Waveguides for Phase-Change Material Devices in SOI Platforms," *Advanced Photonics Congress*, Maastricht, Netherlands, 25-28 July 2022 (DOI: 10.1364/BGPPM.2022.JTu2A.11)
147. L. Réveil, C. Mukherjee, C. Maneux, M. Deng, F. Marc, A. Kumar, G. Larrieu, A. Poittevin, I. O'Connor, O. Baumgartner, D. Pirker, "Analysis of an Inverter Logic Cell based on 3D Vertical NanoWire Junction-Less Transistors," *30th IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SoC 2022)*, Patras, Greece, 3-5 October 2022 (DOI: 10.1109/VLSI-SoC54400.2022.9939576)
148. R. Cardoso, C. Zrounba, M. Abdalla, P. Jimenez, M. Gomes, B. Charbonnier, F. Pavanello, I. O'Connor, S. Le Beux, "Towards a Robust Multiply-Accumulate Cell in Photonics using Phase-Change Materials," *Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, 17-19 April 2023 (DOI: 10.23919/DATE56975.2023.10137313)
149. T. Shahroodi, R. Cardoso, M. Zahedi, S. Wong, A. Bosio, I. O'Connor, S. Hamdioui, "Lightspeed binary neural networks using optical phase-change materials," *Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, 17-19 April 2023 (DOI: 10.23919/DATE56975.2023.10137229)
150. S. Pappalardo, A. Ruospo, I. O'Connor, B. Deveautour, E. Sanchez, A. Bosio, "A Fault Injection Framework for AI Hardware Accelerators," *IEEE Latin-American Test Symposium (LATS)*, Veracruz, Mexico, 21-24 March 2023 (DOI: 10.1109/LATS58125.2023.10154505)
151. S. Pappalardo, A. Ruospo, I. O'Connor, B. Deveautour, E. Sanchez, A. Bosio, "Resilience-Performance Tradeoff Analysis of Deep Neural Network Accelerator," *26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, Tallinn, Estonia, 3-5 May 2023 (DOI: 10.1109/DDECS57882.2023.10139704)
152. R. Cardoso, C. Zrounba, M. Abdalla, P. Jimenez, M. Gomes, B. Charbonnier, F. Pavanello, I. O'Connor, S. Le Beux, "Photonic Convolution Engine Based on Phase-Change Materials and Stochastic Computing," in IEEE Computer

Society Annual Symposium on VLSI (ISVLSI), Foz do Iguacu, Brazil, 20-23 June 2023, (DOI: 10.1109/ISVLSI59464.2023.10238608)

153. A. Piri, S. Pappalardo, S. Barone, M. Barbareschi, B. Deveautour, M. Traiola, I. O'Connor, A. Bosio, "Input-aware accuracy characterization for approximate circuits," *53rd IEEE/IFIP International Conference on Dependable Systems and Networks - 8th Workshop on Approximate Computing (AxC)*, Porto, Portugal, 27 June 2023 (DOI: 10.1109/DSN-W58399.2023.00050)
154. Y. Wang, C. Mukherjee. H. Rezgui, M. Deng, C. Maneux, S. Mannaa, I. O'Connor, J. Müller, S. Pelloquin, G. Larrieu, "Electrothermal modeling of junctionless vertical Si nanowire transistors for 3D logic circuit design," *53rd IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 57-60, Lisbon, Portugal, 2023 (DOI: 10.1109/ESSDERC59256.2023.10268560)
155. C. Zrounba, R. Cardoso, M. Gomes de Queiroz, P. Jimenez, M. Abdalla, A. Bosio, S. Le Beux, F. Pavanello, I. O'Connor, "Introducing SPECS: Scalable Photonic Event-driven Circuit Simulator," *49th European Conference on Optical Communications (ECOC)*, Glasgow, Scotland, 1-5 October 2023 (DOI: 10.1049/icp.2023.2480)
156. S. Pappalardo, A. Piri, A. Ruospo, I. O'Connor, B. Deveautour, A. Bosio, E. Sanchez, "Investigating the effect of approximate multipliers on the resilience of a systolic array DNN accelerator," *36th IEEE Int. Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)*, Juan-Les-Pins, France, 3-5 October 2023
157. M. Gomes de Queiroz, R. Cardoso, M. Abdalla, P. Jimenez, I. O'Connor, A. Bosio, F. Pavanello, "Power Reduction in Photonic Meshes by MZI Optimization," Frontiers in Optics + Laser Science (FiO+LS), Seattle (WA), USA, 9-12 October 2023
158. S. Pappalardo, A. Piri, A. Ruospo, I. O'Connor, B. Deveautour, E. Sanchez, A. Bosio, "Investigating the effect of approximate multipliers on the resilience of a systolic array DNN accelerator," *IEEE Workshop on Automotive Reliability, Test and Safety (ARTS)*, Anaheim (CA), United States, 12-13 October 2023
159. M. Abdalla, M. Gomes, P. Jimenez, R. Cardoso, C. Zrounba, G. Ren, A. Boes, A. Mitchell, A. Bosio, I. O'Connor, Fabio Pavanello, "Exploring the bandwidth-limited readout in coherent photonic reservoir computing," *Int. Conf. Neuromorphic, Natural and Physical Computing (NNPC)*, Hanover, Germany, 25-27 October 2023 (https://nnpc-conference.com/wp-content/uploads/2024/04/Physical-substrates-materials-devices-micro-architectures_Mohab-Abdalla.pdf)
160. R. Cardoso, C. Zrounba, M. Abdalla, P. Jimenez, M. Gomes, B. Charbonnier, F. Pavanello, I. O'Connor, S. Le Beux, "Signed Convolution in Photonics with Phase-Change Materials using Mixed-Polarity Bitstreams," *29th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Incheon, South Korea, 22-25 January 2024 (DOI: 10.1109/ASP-DAC58780.2024.10473952)
161. T. Shahroodi, R. Cardoso, S. Wong, A. Bosio, I. O'Connor, S. Hamdioui, "High-Performance Data Mapping for BNNs on PCM-based Integrated Photonics," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Valencia, Spain, 25-27 March 2024 (DOI: 10.23919/DATE58400.2024.10546687)
162. I. O'Connor, S. Mannaa, A. Bosio, B. Deveautour, D. Deleruyelle, T. Obukhova, C. Marchand, J. Trommer, C. Cakirlar, B. Neckel Wesling, T. Mikolajick, O. Baumgartner, M. Thesberg, D. Pirker, C. Lenz, Z. Stanojevic, M. Karner, G. Larrieu, S. Pelloquin, K. Moustakas, J. Muller, G. Ansaloni, A. Amirshahi, D. Atienza, J.L. Rouas, L. Ben Letaifa, G. Bordea, C. Brazier, Y. Wang, C. Mukherjee, M. Deng, M. François, H. Rezgui, L. Reveil, C. Maneux, "The 3D Neural Network Compute Cube (N2C2) Concept enabling Efficient Hardware Transformer Architectures towards Speech-to-Speech Translation," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Valencia, Spain, 25-27 March 2024 (DOI: 10.23919/DATE58400.2024.10546700)
163. S. Mannaa, C. Marchand, D. Deleruyelle, B. Deveautour, A. Bosio, C. Lenz, O. Baumgartner, I. O'Connor, "3D VNWFET-Based Standard Cell Library Design Flow: from Circuit and Physical Design to Logic Synthesis," *32nd IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Tanger, Morocco, 6-9 October 2024 (DOI: 10.1109/VLSI-SOC62099.2024.10767812)
164. L. Rhétat, J.P. Noël, B. Giraud, L. Grenouillet, J. Laguerre, C. Marchand, I. O'Connor, "A Novel Design Technique for Enhanced Security and New Applications of Ferroelectric-based Non-Volatile SRAM," *32nd IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Tanger, Morocco, 6-9 October 2024 (DOI: 10.1109/VLSI-SOC62099.2024.10767797)
165. M. Gomes de Queiroz, M. Vidaletti Costa, P. Jimenez, I. O'Connor, A. Bosio, F. Pavanello, "Unfair Photonics? How Encoding May Lead to Bias in Photonic Neural Networks," Conference on Lasers and Electro-Optics (CLEO), 4 May 2025, Long Beach (CA), United States

166. S. Pelloquin, J. Muller, S. Mannaa, I. O'Connor, G. Larrieu, "Scalable 3D Logic Cells Using Vertical Sub-20 Nm Gate-All-Around Nanowire FETs for High-Density Integration," *247th Electrochemical Society (ECS) Meeting*, Montreal, Canada, 18-22 May 2025
167. J. Martinez, N. Bhattacharjee, Y. He, G. Galderisi, I. O'Connor, T. Mikolajick, J. Trommer, "Bi-Linearity of Back Gated Schottky Barrier Transistors on an Industrial 22nm FDSOI Platform for Efficient In-Hardware Matrix-Vector Multiplication and Addition," *23rd IEEE International NEWCAS Conference*, 22-25 June 2025, Paris, France
168. S. Pelloquin, A. Kumar, S. Mannaa, J. Müller, K. Moustakas, O. Baumgartner, I. O'Connor, G. Larrieu, "Scaled Vertical Transport Gate-All-Around Nanostructured Channel (Nanosheet/Nanowire) Technology for Advanced CMOS Devices", *IEEE European Solid-State Electronics Research Conference (ESSERC)*, 8-11 September 2025, Munich, Germany
169. M. Filsinger, A. Cauquil, D. Deleruyelle, D. Navarro, I. O'Connor, C. Marchand, "On the Possibility of Relying Solely on FeMFET Variability for PUF Implementations," *33rd IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Puerto Varas, Chile, 12-15 October 2025
170. B. Darne, M. Filsinger, A. Bosio, D. Deleruyelle, I. O'Connor, B. Vilquin, C. Marchand, "Non-volatile Ferroelectric-AND (FeAND) memory cell design," *33rd IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Puerto Varas, Chile, 12-15 October 2025
171. R. Pronsato, A. Cauquil, P. Vivet, J. Coignus, D. Deleruyelle, C. Marchand, A. Bosio, L. Labrak, I. O'Connor, "Exploring Enhancements of 1T1C FeMFET Bitcell With a Versatile DTCO Methodology," *33rd IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Puerto Varas, Chile, 12-15 October 2025 **(Recipient of Best Paper Award)**
172. M. Vidaletti Costa, M. Gomes de Queiroz, R. Cardoso, I. O'Connor, A Mitchell, "Noise and Quantization Parameterization of Photonic Convolution Accelerator," *33rd IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Puerto Varas, Chile, 12-15 October 2025
173. M. Vidaletti Costa, M. Gomes de Queiroz, R. Cardoso, I. O'Connor, A. Mitchell, "Zeros, Negatives, and Fewer Bits: Stress-Testing a Photonic Convolutional Neural Network," *IEEE Photonics Global Conference (PGC)*, Sanya, China, 5-8 December 2025
174. M. Gomes de Queiroz, L. Alexandrino de Melo, M. Vidaletti Costa, S. Pappalardo, F. Pavanello, I. O'Connor, A. Bosio, "Case Study: Improving the Robustness of Photonic Neural Networks Against Memory Faults," *IEEE 27th Latin American Test Symposium (LATS)*, Florianopolis, Brazil, March 17-20 2026
175. T. Spyrou, K. Stavrakakis, Y. Biyani, R. Bishnoi, S. Hamdioui, J. Minguet Lopez, L. Dumas, J. Coignus, D. Ly, Hugo Chazot-Ranquet, L. Grenouillet, F. Grimaud, S. Martin, O. Billoint, F. Andrieu, R. Alcala, S. Slesazeck, A. Sunil, C. Peng, A. Cauquil, R. Pronsato, D. Deleruyelle, C. Marchand, A. Bosio, I. O'Connor, G. Urlini, S. Jeannot, M. Sajedi, A. Nima, A. Moghaddam, T. Werner, T. Schenk, B. Cheng, M. Khoei, L. Perez Ramírez, E. Koh, S. Kale, N. Barrett, "Multi-Partner Project: Scalable, Ferroelectric-based Accelerators for Energy Efficient Edge AI (Ferro4EdgeAI)," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Verona, Italy, 20-22 April 2026
176. H. Benamara, S. Ait Belkacem, M. Ramirez-Corrales, L. Ciampolini, J.P. Noel, M. Kooli, L. Ammoura, I. O'Connor, P. Girard, A. Virazel, "Enhancing Testability & Security of Near-Memory Computing Architectures," *44th IEEE VLSI Test Symposium (VTS)*, Napa (CA), USA, 27-29 April 2026 (DOI: 10.1109/vts69484.2026.11563203)
177. L. Rhétat, J.P. Noël, B. Giraud, L. Grenouillet, C. Marchand, I. O'Connor, "A Ferroelectric nvSRAM PUF with Built-In Grey Bit Masking based on FeCAP-SRAM Interactions," *IEEE 31st European Test Symposium (ETS)*, Chania, Greece, 25-29 May 2026
178. S. Mannaa, G. Loubet, S. Pappalardo, C. Marchand, D. Deleruyelle, A. Bosio, C. Lenz, O. Baumgartner, Y. Wang, F. Marc, C. Mukherjee, C. Maneux, I. O'Connor, "A Holistic Framework to Assess Reliability Issues in Emerging Technologies due to Ageing, Voltage and Temperature Variation," *IEEE 31st European Test Symposium (ETS)*, Chania, Greece, 25-29 May 2026
179. A. Cauquil, R. Pronsato, M. Filsinger, J. Minguet-Lopez, J. Coignus, D. Deleruyelle, I. O'Connor, "Process and layout-Aware Reliability Analysis of FeMFET Crossbar Linearity," IEEE 24th Interregional NEWCAS Conference, Chicoutimi, Canada, June 21-24, 2026
180. H. Benamara, M. Kooli, L. Ciampolini, T. Bricout, P. Vivet, I. O'Connor, "Energy-Aware Fast and Accurate Design Space Exploration of Near-Memory Computing," *34th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Limassol, Cyprus, 11-14 October 2026

181. C. Marchand, M. Filsinger, I. O'Connor, S. Slesazeck and T. Mikolajick, “Side-channel aware design of FeFET based memory for cryptographic SBox implementation,” *34th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Limassol, Cyprus, 11-14 October 2026
182. R. Pronsato, A. Cauquil, M. Filsinger, D. Deleruyelle, I. O'Connor, “Surrogate-assisted DTCO for 1T1C FeMFET Bitcells: A Comparative Study on Model Choice and Data Sampling,” *34th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Limassol, Cyprus, 11-14 October 2026
183. L.M. Wisniewski, F. Melul, J.D. Aguirre-Morales, M. Bocquet, D. Deleruyelle, I. O'Connor, L. Dumas, J. Coignus, L. Grenouillet, J. Minguet Lopez, J.M. Portal, “A Comprehensive Analysis of FemFET Retention,” IEEE International Integrated Reliability Workshop (IIRW), South Lake Tahoe (CA), USA, 4-8 October 2026

Workshops, seminars, tutorials and panel discussions

1. I. O’Connor, A. Kaiser, "Synthèse de circuits à courants commutés," *Colloque CAO de Circuits Intégrés et Systèmes*, Villard de Lans, 1997, p. 2-5
2. G. Jacquemod, I. O'Connor, F. Gaffiot, "Microelectronics education and research at Ecole Centrale de Lyon," *SAME 98*, Sophia Antipolis, October 29th 1998
3. F. Mieyeville, F. Gaffiot, I. O'Connor, G. Jacquemod, "Modélisation comportementale de liens optiques pour des interconnexions à courte distance," *Colloque CAO de Circuits Intégrés et Systèmes*, Aix en Provence, 1999, p. 209-212
4. F. Gaffiot, G. Jacquemod, P. Bontoux, F. Mieyeville, I. O'Connor, "Behavioral modeling of photonic and optronic systems," *2nd CFDRC Workshop on MEMS Simulation Technology*, Berlin, June 1999
5. F. Mieyeville, G.Jacquemod, F.Gaffiot, I. O'Connor, "Modèle thermo-opto-électronique de VCSEL pour la simulation de liens optiques pour des interconnexions à courte distance," *3émes Journées Nationales du Réseau Doctoral de Microélectronique*, Montpellier, 4-5 Mai 2000
6. F. Mieyeville, F.Gaffiot, I. O'Connor, G.Jacquemod, "Modélisation d'un lien optique inter et intra puce à haut débit," *11èmes Rencontres Régionales de la Recherche*, Saint Etienne, 20 septembre 2000
7. M. Brière, F. Gaffiot, I. O'Connor, F. Mieyeville, "Modélisation comportementale d’un détecteur de fluorescence," *7èmes Journées Pédagogiques du CNFM*, Saint Malo, novembre 2002
8. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, F. Gaffiot, "Sur l’utilisation de la logique floue dans la synthèse de circuits analogiques," *7èmes Journées Pédagogiques du CNFM*, Saint Malo, novembre 2002
9. F. Mieyeville, F. Gaffiot, I. O'Connor, J. Oudinot, P. Raynaud and F Mkalech, "VCSEL-based Optical Communication Link Simulation using VHDL-AMS," DATE 2003, Exhibition Forum, Session X
10. I. O'Connor, "Le Laboratoire d'Electronique, Optoélectronique et Microsystèmes de l'Ecole Centrale de Lyon," *Escola Polytechnica de l'Université de Sao Paolo*, 12 septembre 2003
11. M. Brière, F. Mieyeville, I. O’Connor and F. Gaffiot, "Un réseau d’interconnexion optique passif basé sur le routage en longueur d’onde," Symposium en Architecture et Adéquation Algorithme Architecture, pp. 425-432, La Colle-sur-Loup, France, 15-17 octobre 2003
12. I. O'Connor, "Interconnexions Optiques Intégrées," *Action Spécifique "SOC et Nouvelles Technologies" (RTP SOC)*, Paris, 10 décembre 2003
13. E. Belhaire, P. Desgreys, P. Fouillat, P. Garda, Y. Hervé, I. O'Connor, "Présentation finale de l'Action spécifique SOC AMS," *Workshop RTP SOC*, La Londe les Maures, 18 mai 2004
14. E. Belhaire, N. Drach-Temam, P. Garda, I. O'Connor, "Présentation de l'Action Spécifique SOC et Nouvelles Technologies," *Workshop RTP SOC*, La Londe les Maures, 18 mai 2004
15. E. Drouard, M. Brière, X. Letartre, F. Mieyeville, I. O’Connor, F. Gaffiot, "Modélisation phénoménologique de réseaux WDM sur puce," Journées Nationales d’Optique Guidée, Paris, octobre 2004
16. M. Brière, T. Michalke, I. O’Connor, F. Mieyeville, D. Navarro, F. Gaffiot, "Modélisation de composants photoniques sous Matlab et VHDL-AMS pour la simulation de réseaux optiques sur puce," 8èmes Journées Pédagogiques du CNFM, Saint Malo, décembre 2004
17. M. Le Helley, F. Mieyeville, D. Navarro, I. O’Connor, "Conception d’un microprocesseur RISC," 8èmes Journées Pédagogiques du CNFM, Saint Malo, décembre 2004
18. I. O'Connor, "Interconnexions optiques intégrées," *Séminaire LIRMM*, Montpellier, 11 février 2005
19. I. O'Connor, "Heterogeneous Systems on Chip: Design methodologies and integrated optical interconnect," *Séminaire* ReSMiQ, Ecole Polytechnique de Montréal (QC), Canada, 5 décembre 2005

20. I. O'Connor, F. Tissafi-Drissi, D. Navarro, F. Mieyeville, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, D. Van Thourhout, "Optical interconnect for on-chip data communication" (invited), *DATE Workshop on Future Interconnect and Networks on Chip*, Munich, Germany, 10 March 2006
21. W. Heirman, J. Dambre, I. O'Connor, J. Van Campenhout, "Reconfigurable Optical Networks for On-Chip Multiprocessors," *DATE Workshop on Future Interconnect and Networks on Chip*, Munich, Germany, 10 March 2006
22. I. O'Connor, P. Garda, "Plate-forme STIC RFVSOC," *3ème workshop CNRS RECAP*, Lyon, 17 November 2006
23. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Reconfigurable computing with emerging devices," *Keio-ECL Nanoworkshop*, Ecully, 24 November 2006
24. I. O'Connor, "Gate-level reconfigurability using asymmetric double-gate MOSFET devices," *Keio-ECL Nanoworkshop*, Yokohama, 5 November 2007
25. I. O'Connor, "Conception de cellules reconfigurables à base de composants avancés et émergents," *Séminaire L2MP*, Marseille, 6 décembre 2007
26. I. O'Connor, "Reconfigurable cells based on advanced and emerging double gate devices," *Séminaire ReSMiQ*, Ecole Polytechnique de Montréal (QC), Canada, 18 January 2008
27. I. O'Connor, D. Van Thourhout, J.M. Fedeli, "Process and design technology for on-chip optical interconnect," *Int. VLSI/ULSI Multilevel Interconnection Conference*, 27-30 October 2008, Fremont (CA), USA
28. I. O'Connor, "Optical interconnect for future systems on chip," *Séminaire ETIS*, Paris, 3 février 2009
29. I. O'Connor, "Logic architectures with emerging technologies," *MSc Erasmus Tutorial*, TU Lodz, 21 June 2009
30. I. O'Connor, Panel on "Evolution or Revolution of the Microprocessor Era needed?", *17th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 12-14 2009, Florianopolis, Brazil
31. I. O'Connor, "Architectures reconfigurables à l'échelle nanométrique", Atelier "De la modélisation des nano-dispositifs aux circuits innovants'', GDRs SoC-SiP / Nanoélectronique, Bordeaux, 9-11 December 2009
32. F. Frantz, L. Labrak, I. O'Connor, "Methods and Tools for 3D Heterogeneous Design", *DATE'10 Friday Workshop on 3D Integration*, pp. 52-53, Dresden, Germany, 12 March 2010
33. I. O'Connor, "Architectures de calcul à base de technologies émergentes," *Séminaire RQMP*, U. Sherbrooke (QC), Canada, 25 June 2010
34. I. O'Connor, "Emerging technologies and nanoscale computing fabrics, *Séminaire LabSTICC*, Brest, 6 December 2010
35. O. Valorge, M. Rousseau, F. Calmon, C. Gontrand, T. Lacrevaz, A. Farcy, J. Charbonnier, C. Fuchs, I. O'Connor, L. McIlrath, "Digital Signal Propagation in 3D Passive Interposer Interconnections," *DATE'11 Friday Workshop on 3D Integration*, Grenoble, France, 18 March 2011
36. F. Frantz, L. Labrak, I. O'Connor, "A meta-optimization approach to setup a 3D thermal-aware floorplanner," *DATE'11 Friday Workshop on 3D Integration*, Grenoble, France, 18 March 2011
37. J. Xu, I. O'Connor, J. Kim, KAIST, "Optical Network-on-Chip: An Emerging Technology for Energy-Efficient Multi-Core Systems," *Tutorial, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Hong Kong, China, 2 October 2011
38. I. O'Connor, "Emerging technologies and nanoscale computing fabrics", *Hong Kong University of Science and Technology Seminar*, Hong Kong, 6 October 2011
39. I. O'Connor, "Défi Nouveaux Paradigmes - Towards hybrid neuro-reconfigurable computing," *Colloque CNRS-G3N*, Paris, 12 November 2012
40. I. O'Connor, "Emerging Technologies and Architectures for Green Computing," *Journée ARC6*, Grenoble, 22 November 2012
41. F. Frantz, D. Matos, L. Labrak, F. Clermidy, I. O'Connor, L. Carro, A. Susin, "MoNICA: Performance- and Thermal-Aware Floorplan for Heterogeneous 3D NoC-based MPSoCs," *DATE'13 Friday Workshop on 3D Integration*, Grenoble, France, 22 March 2013
42. I. O'Connor, K. Jabeur, S. Le Beux, D. Navarro, "Ambipolar logic circuit design and synthesis," *Functionality-Enhanced Devices Workshop (FED)*, Lausanne, Switzerland, 25 March 2013
43. S. Le Beux, I. O'Connor, "Auto-reconfiguration in statically interconnected CNTFET-based cells," *Functionality-Enhanced Devices Workshop (FED)*, Lausanne, Switzerland, 25 March 2013
44. I. O'Connor, "Optical Network-on-Chip: An Emerging Technology for Energy-Efficient Multi-Core Systems," MIGAS Summer School, Autrans, 24-28 June 2013

45. I. O'Connor," Five Grand Challenges for Circuits in Emerging Nanotechnologies," *Panel on Circuits in Emerging Technologies*, *Symposium on Emerging Trends in Electronics* (http://www.nano-tera.ch/events/lyrical.php?callsign=panelcircuits), Montreux, Switzerland, 1-2 December 2014
46. I. O'Connor, "Position statement," *Panel on Critical research areas driven by industry transformations*, *Design Automation and Test in Europe (DATE) 2015*, Grenoble, France, 9-13 March 2015
47. I. O'Connor, "The Last Mile? Remaining Challenges in Optical Interconnect," DATE'15 International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS), Grenoble, France, 13 March 2015
48. J. Luo, D. Chillet, C. Killian, S. Le Beux, I. O'Connor, O. Sentieys, "Crosstalk noise aware wavelength allocation in WDM 3D ONoC," *Colloque National du GDR SoC-SiP*, 8-10 June 2016, Nantes, France
49. V.D. Pham, D. Chillet, C. Killian, S. Le Beux, I. O'Connor, O. Sentieys, "Gestion de la consommation d'un ONoC intégré dans un MPSoC," *Colloque National du GDR SoC-SiP*, 8-10 June 2016, Nantes, France
50. P. Van Dung, C. Killian, D. Chillet, S. Le Beux, O. Sentieys, I. O'Connor, "Gestion de la consommation d'un réseau optique intégré dans un MPSoC," *Conférence d'informatique en Parallélisme, Architecture et Système (COMPAS)*, Lorient, France, 5-8 July 2016
51. J. Luo, D. Chillet, C. Killian, S. Le Beux, I. O'Connor, O. Sentieys, "Wavelength spacing optimization to reduce crosstalk in WDM 3D ONoC," *Conférence d'informatique en Parallélisme, Architecture et Système (COMPAS)*, Lorient, France, 5-8 July 2016
52. I. O'Connor, "Position statement," *Panel on Horizon 2050: Chip Design in 35 years from now*, *24th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, Tallinn, Estonia, 26-28 September 2016
53. I. O'Connor, "Optical Interconnect Technology & Design Roadmap," *Nereid Domain Workshop - Connectivity*, Bertinoro, Italy, 17-21 October 2016
54. I. O'Connor, "How the miracle of nanotechnology has brought us into the information age," *TEDxEMLyon Miraculous in the Common*, Lyon, France, 17 November 2016
55. V.D. Pham, D. Chillet, C. Killian, O. Sentieys, S. Le Beux, I. O'Connor, "Interface Electrique/Optique pour un ONoC," *Colloque GRETSI*, Juan-Les-Pins, France, 5-8 September 2017
56. I. O'Connor, "Synthesis and DSE techniques for matrix-based ambipolar logic architectures," *Workshop on Logic Synthesis and Emerging Technologies*, Lausanne, Switzerland, 28-29 September 2017
57. I. O'Connor, "Multi-scale Photonic Interconnect Solutions," *IRT-Nanoelec Workshop National "Photonique sur Silicium"*, Paris, France, 27 novembre 2017
58. I. O'Connor, "Multi-Scale Photonic Interconnect Solutions," *Post Moore Interconnects Workshop / ISC*, Frankfurt, Germany, 28 June 2018
59. I. O'Connor, "Laser Group Control for Efficient Thermal-Aware Calibration of Nanophotonic Interconnects," Workshop on Design for 3D Silicon Integration (D43D), Grenoble, France, 2-3 July 2018
60. I. O'Connor, "Position statement," *Panel on Computation-in-Memory: Hype or Hope? IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Verona, Italy, 8-10 October 2018
61. F. Maraninchi, A. Rhouni, I. O'Connor, E. Kerhervé, M.M. Louerat, L. Bossuet, P. Nouet, A. Pinna, M. Pala, N. Dehaese, "Initiative Microélectronique - GT 1 : Conception/Architectures/Logiciels/Systèmes embarqués - Synthèse intermédiaire," Séminaire Microélectronique CNRS, Meudon, France, 14 December 2018
62. I. O'Connor, "Quo vadis ICT? Information and communication technologies - Challenges, perspectives and INL," Lyon, France, 17 January 2019
63. I. O'Connor, "Position statement," Panel on Bringing on-Chip Optical Interconnects into the Real World, DATE'19 International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS), Florence, Italy, 29 March 2019
64. I. O'Connor, M. Cantan, L. Mozzone, C. Marchand, A. Bosio, D. Deleruyelle, "Granularity Exploration for Logic in Memory," Phase Change Workshop, Villars sur Ollon, Switzerland, 14th January 2020
65. I. O'Connor, M. Cantan, L. Mozzone, C. Marchand, A. Bosio, S. Le Beux, D. Deleruyelle, "Opportunities for non-volatile ferroelectric logic in edge computing," Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes (FETCH), Montreal, QC (CA), 12-14 February 2020
66. I. O'Connor, Z. Stanojevic, O. Baumgartner, C. Mukherjee, G. Larrieu, J. Trommer, C. Maneux, "Analysis of Energy-Delay-Product for a 3D Vertical Nanowire FET Technology for Logic Applications," 2nd June 2020, hal-02732902
67. I. O'Connor, A. Poittevin, A. Bosio, S. Le Beux, C. Marchand, G. Larrieu, C. Maneux, "Vertical nanowire FETs and their impact on 3D computing architectures," *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)*, Salt Lake City (UT), USA, 5-9 October 2020

68. E. Dupuis, D. Novo, I. O'Connor, A. Bosio, "Fast exploration of weight sharing opportunities for CNN compression," *DATE 2021 Friday Workshop on System-level Design Methods for Deep Learning on Heterogeneous Architectures (SLOHA 2021)*, Grenoble (virtual), France, 5th February 2021
69. C. Maneux, D. Atienza, A. Levisse, G. Ansaloni, O. Baumgartner, Z. Stanojevic, A. Bosio, I. O'Connor, G. Larrieu, J. Trommer, M. Deng, G. Bordea, C. Mukherjee, J.L. Rouas, "How novel technologies can boost neuromorphic computing? A view from European project consortia," (invited), *Workshop NEUROTECH*, virtual, 27 April 2021
70. C. Maneux, C. Mukherjee, M. Deng, M. Dubourg, L. Reveil, G. Bordea, A. Lecestre, G. Larrieu, J. Trommer, E.T. Breyer, S. Slesazeck, T. Mikolajick, O. Baumgartner, M. Karner, D. Pirker, Z. Stanojevic, David A. Atienza, A. Levisse, G. Ansaloni, A. Poittevin, A. Bosio, D. Deleruyelle, C. Marchand, I. O'Connor, "Why neuromorphic computing need novel 3D technologies? A view from FVLLMONTI European project consortium," (invited), *High Performance Embedded Architecture and Compilation (HiPEAC) Computing Systems Week (CSW)*, Lyon, France, 25-27 October 2021
71. I. O'Connor, "Ferroelectric-enabled energy-efficient non-volatile edge computing," *In-Memory Architectures and Computing Applications Workshop (iMACAW @ DAC 2022)*, San Francisco, USA, 10 July 2022
72. I. O'Connor, "Ferroelectric-enabled energy-efficient non-volatile edge computing," *Mondays in Memory (MiM – In-Memory Computing Webinar Series)*, TU Wien (virtual), Austria, 16 October 2022
73. I. O'Connor, "Emerging technology based 3D compute cubes for edge intelligence", *IEEE CASS Talks*, UFRGS (virtual), Brazil, 25 November 2022
74. I. O'Connor, "Silicon photonics platforms: from communication to computing," *Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes (FETCH)*, Lavey-les-Bains, Switzerland, 1-3 February 2023
75. C. Maneux, M. Deng, C. Mukherjee, D. Atienza, J. Trommer, O. Baumgartner, G. Larrieu, I. O'Connor, "Emerging technology and new computing paradigms: How to reinvent the value chain?" *Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes (FETCH)*, Lavey-les-Bains, Switzerland, 1-3 February 2023
76. P.A. Matrangolo, S. Mannaa, C. Marchand, D. Navarro, A. Bosio, I. O'Connor, "Electrical Characterization of Emerging Technologies of Transistor," *In-Memory Architectures and Computing Applications Workshop (iMACAW @ DAC 2023)*, San Francisco (CA), USA, 9 July 2023
77. I. O'Connor, D. Atienza, J. Trommer, O. Baumgartner, G. Larrieu, C. Maneux, "Emerging technology-based 3D compute cubes for edge intelligence," *X-GDR BarCamp sur les Défis d'Implémentation de l'IA : Sécurité, Fiabilité, Soutenabilité et Nouvelles Technologies*, Aussois, 13-15 December 2023
78. I. O'Connor, "Next-Gen AI Hardware: Shaping the Datacenter Revolution," *LID World Summit 2025 – AI Transforming HPC & Data Centers*, 18 June 2025, Grenoble, France
79. I. O'Connor, "Position statement," Panel on Navigating the tides of funding for chips and system design, *Design Automation Conference*, San Francisco (CA), USA, 22-25 June 2025
80. I. O'Connor, "Next-Gen AI Hardware in Datacenters: Energy-Efficiency and other stories," *ECL Alumni Ignite*, London, UK, 8 October 2025
81. B. Gayral, I. O'Connor, C. Théard-Jallu, "Technologies émergentes : nanotechnologies, quantique, ADN… les promesses de la recherche en matière de réduction de l'impact environnemental et d'efficacité énergétique," GreenTech Forum, Paris, France, 4-5 November 2025
82. I. O'Connor, "Building Energy-Efficient, High-Performance Circuits and Architectures Tailored to Machine Learning Computation," Lecture, Advanced School on AI and Intelligent Systems: Design, Engineering, and Architectures, Favignana (Sicily), Italy, 8-11 June 2026
83. I. O'Connor, invited talk, NEUROCOM Workshop, HiPEAC 2027 Conference, Glasgow, United Kingdom, January 2027 (forthcoming)

Press and science outreach publications

1. I. O'Connor, "Voyage au cœur des technologies de fabrication pour la réalisation des futurs systems of systems-on-chip, des systèmes embarqués et des objets connectés," Télécom, no. 205, pp. 8-10, juin 2022
2. J.L. Rouas, G. Ansaloni, I. O'Connor, O. Baumgartner, G. Larrieu, J. Trommer, C. Maneux, "Putting AI in your Ears with 3D Neural Networks," Scientia Global Engineering & Computing, 1310, August 2025 (doi: 10.33548/SCIENTIA1310)

3. [interview cited by] L. Allen, "Government Funding For Chip Design Tools Spreads," Semiconductor Engineering, August 2025 (https://semiengineering.com/government-funding-for-chip-design-tools-spreads/)
4. [interview cited by] P. Brans, "Could NTT's Low-Power Chip Be a Game Changer for Drones?," EE Times, November 2025 (https://www.eetimes.com/could-ntts-low-power-chip-be-a-game-changer-for-drones/)
5. M. Holive, I. O'Connor, "The Hidden Energy Drain Behind AI and What We Can Do About it" Proteus Leader Show, November 2025 (https://www.linkedin.com/posts/marieholive_did-you-know-a-single-chatgpt-query-uses-activity-7391103031586746368-Gxvf/)
6. [interview cited by] P. Brans, "Europe's Chips Act Stumbles Over Its Own Rigidity," EE Times, November 2025 (https://www.eetimes.eu/europes-chips-act-stumbles-over-its-own-rigidity/)
7. I. O'Connor, "The Co-Optimized Silicon Stack," ongoing weekly series on the future of chip technology, LinkedIn, since August 2026 (14 articles to date) (https://www.linkedin.com/in/ian-o-connor-7592153/)

Patents

1. I. O'Connor, I. Hassoune, "Cellule logique reconfigurable à base de transistors MOSFET double grille," *Brevet français* n° 07 56487 (extension EU, USA), 13 juillet 2007
2. P.E. Gaillardon, F. Clermidy, I. O'Connor, P.H. Morel, "Cellules booléennes reconfigurables à matrice de nanofils entrecroisés," *Brevet français* n° 09 58894, WO2011070164 PCT, 11 décembre 2009
3. N. Yakymets, I. O'Connor, "Matrice topologie croisée," *Brevet français* n° 09 58957, 14 décembre 2009
4. K. Jabeur, I. O'Connor, "Porte logique statique programmable à transistors ambipolaires et équipement électronique associé," *Brevet français* n° 10 59363, 15 novembre 2010
5. K. Jabeur, I. O'Connor, "Porte logique dynamique programmable," *Brevet français* n° 10 59364, 15 novembre 2010
6. I. O'Connor, L. Labrak, F. Frantz, "Procédé de conception optimisée de circuits électroniques intégrés," *Brevet français* n° 11 61180, 5 décembre 2011
7. S. Le Beux, I. O'Connor, "Interface reconfigurable pour réseau optique sur puce," Brevet français, 2014

Theses

1. I. O'Connor, "Josephson contact based digital-analog converter structures," *Diplomarbeit*, Universität Karlsruhe (D), 1992, 82 p.
2. I. O'Connor, "Automated design of switched-current cells," *Thèse de doctorat*, Université de Lille I, 1997, 224 p.
3. I. O'Connor, "Systèmes sur puce physiquement hétérogènes : Méthodologies de conception et Systèmes optiques d'interconnexion," *Habilitation à Diriger des Recherches*, Ecole Centrale de Lyon, 2005, 142 p.

Conference organization

Conference Name	*Dates*	*Place*	*Role*
OWTNM 2005 (Optical Waveguide Theory and Numerical Modeling) / ECIO 2005 (European Conference on Integrated Optics)	6th-8th April 2005	Grenoble, France	Session chair (Modeling of integrated and nanophotonics devices I) TPC member
DATE 2006 (Design Automation and Test in Europe)	6th-10th March 2006	Munich, Germany	TPC member (Analog and Mixed-Signal Systems and Circuits)
FETCH 2007 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	10th-12th January 2007	Villard de Lans, France	Co-founder, Program Chair
DATE 2007 (Design Automation and Test in Europe)	16th-20th April 2007	Nice, France	Special session Organizer and chair (Heterogeneous Systems on Chip and Systems in Package)
ISIE 2007 (IEEE International Symposium on Industrial Electronics)	4th-7th June 2007	Vigo, Spain	TPC member
ReCoSoC 2007 (Workshop on Reconfigurable Communication-centric Systems-on-Chip)	18th-20th June 2007	Montpellier, France	Session Chair (NoC Architectures) TPC member
TAISA 2007 (Traitement Analogique de l'Information, du Signal et ses Applications)	18th-19th October 2007	Lyon, France	General chair
FETCH 2008 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	7th-9th January 2008	Montebello, QC, Canada	Program Chair
ISVLSI 2008 (IEEE International Symposium on VLSI)	7th-9th April 2008	Montpellier, France	Program Chair Session Chair (Heterogeneous System Design, Nanoscale Circuits) TPC member
NEWCAS 2008 (IEEE Northeast Workshop on Circuits and Systems)	22nd-25th June 2008	Montreal, QC, Canada	Special session organizer and chair (Design Technology for Heterogeneous Systems I) TPC member, Track chair (Mathematical Methods and Design Tools)
ENICS 2008 (International Conference on Advances in Electronics and Micro-electronics)	29th September – 4th October 2008	Valencia, Spain	TPC member
FETCH 2009 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	12th-14th January 2009	Chexbres, Switzerland	Program Chair
DDECS 2009 (IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems)	15th-17th April 2009	Liberec, Czech Republic	TPC member
NEWCAS 2009 (IEEE International New Circuits and Systems Conference)	28th June-1st July 2009	Toulouse, France	Special session organizer and chair (System Level Design for Embedded Systems) TPC member, Special sessions co-chair, Track chair (Mathematical Methods and Design Tools)
FETCH 2010 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	11th-13th January 2010	Chamonix, France	General Chair
DATE 2010 (Design Automation and Test in Europe)	8th-12th March 2010	Dresden, Germany	Session chair (Variability and Yield in Analogue and Mixed-Signal Design) TPC member (Analog and Mixed-Signal Systems and Circuits)
GLSVLSI 2010 (Great Lakes Symposium on VLSI)	16th-18th May 2010	Providence, RI, USA	Track chair (Emerging Technologies) TPC member
ReCoSoC 2010 (International Workshop on Reconfigurable Communication-centric Systems-on-Chip)	17th-19th May 2010	Karlsruhe, Germany	TPC member
VARI 2010 (European Workshop on CMOS Variability)	26th-27th May 2010	Montpellier, France	TPC member
ISCAS 2010 (IEEE International Symposium on Circuits and Systems)	30th May – 2nd June 2010	Paris, France	Special session organizer and chair (On-Chip Optical Interconnect for Manycore Computing Architectures)

Conference Name	*Dates*	*Place*	*Role*
DAC 2010 (Design Automation Conference)	13th-18th June 2010	Anaheim (CA), USA	TPC member (Emerging Technologies)
NEWCAS 2010 (IEEE International New Circuits and Systems Conference)	20th-23rd June 2010	Montreal, QC, Canada	Session chair (CAD and Design Tools) TPC member, Tutorials co-chair, Track chair (Mathematical Methods and Design Tools)
VLSI-SoC 2010 (IFIP/IEEE International Conference on Very Large Scale Integration)	27th-29th September 2010	Madrid, Spain	Topic chair (Green Computing)
ICECS 2010 (IEEE International Conference on Electronics, Circuits, and Systems)	12th-15th December 2010	Athens, Greece	Special session organizer and chair (Designing at the nanoscale: status and perspectives)
FETCH 2011 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	5th-7th January 2011	Quebec, QC, Canada	Steering committee member
DATE 2011 (Design Automation and Test in Europe)	14th-18th March 2011	Grenoble, France	Session co-chair (Design and Simulation of Mixed-Signal Systems) TPC member (Analog and Mixed-Signal Systems and Circuits)
GLSVLSI 2011 (Great Lakes Symposium on VLSI)	2nd-4th May 2011	Lausanne, Switzerland	Track chair (Emerging Technologies) TPC member
FTFC 2011 (Faible Tension Faible Consommation)	30th May – 1st June 2011	Marrakech, Morocco	TPC member
VARI 2011 (European Workshop on CMOS Variability)	30th-31st May 2011	Grenoble, France	TPC member
DAC 2011 (Design Automation Conference)	5th-9th June 2011	San Diego (CA), USA	Session chair (Novel design and analysis tools for emerging devices) TPC member (Emerging Technologies)
Nanoarch 2011 (IEEE/ACM International Symposium on Nanoscale Architectures)	8th-9th June 2011	San Diego, CA, USA	Program Chair, Session chair (Nanofabric updates)
ReCoSoC 2011 (International Workshop on Reconfigurable Communication-centric Systems-on-Chip)	20th-22nd June 2011	Montpellier, France	TPC member
NEWCAS 2011 (IEEE International New Circuits and Systems Conference)	26th-29th June 2011	Bordeaux, France	Session chair (Analog Amplifiers and Voltage References) TPC member, Publicity co-chair, Track chair (CAD and Design Tools)
VLSI-SoC 2011 (IFIP/IEEE International Conference on Very Large Scale Integration)	3rd-5th October 2011	Hong Kong, China	Special session organizer and chair (Emerging Technologies for Networks on Chip) TPC member (track 3-D integration, physical design, compact modeling, electromagnetic analysis)
FETCH 2012 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	9th-11th January 2012	Alpe d'Huez, France	Steering committee member, Steering Committee Liaison chair
DATE 2012 (Design Automation and Test in Europe)	12th-16th March 2012	Dresden, Germany	TPC member (Emerging Technologies, Systems and Applications)
GLSVLSI 2012 (Great Lakes Symposium on VLSI)	3rd-4th May 2012	Salt Lake City, UT, USA	Track chair (Emerging Technologies) TPC member
DAC 2012 (Design Automation Conference)	3rd-7th June 2012	San Francisco (CA), USA	TPC member (Emerging Technologies)
VARI 2012 (European Workshop on CMOS Variability)	11th-12th June 2012	Nice, France	TPC member
NEWCAS 2012 (IEEE International New Circuits and Systems Conference)	17th-20th June 2012	Montreal (QC), Canada	TPC member, Track chair (CAD and Design Tools)
Nanoarch 2012 (IEEE/ACM International Symposium on Nanoscale Architectures)	4th-6th July 2012	Amsterdam, NL	Finance Chair, TPC member Session chair (Neural computing)
VLSI-SoC 2012 (IFIP/IEEE International Conference on Very Large Scale Integration)	7th-10th October 2012	Santa Cruz (CA), USA	Topic co-chair (2D- and 3D-interconnect architectures and topologies including NoCs)
ICECS 2012 (IEEE International Conference on Electronics, Circuits, and Systems)	9th-12th December 2012	Seville, Spain	Track chair (Emerging Technologies – Nano, MEMs), TPC member

Conference Name	*Dates*	*Place*	*Role*
FETCH 2013 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	7th-9th January 2013	Leysin, Switzerland	Steering committee member
DATE 2013 (Design Automation and Test in Europe)	18th-22nd March 2013	Grenoble, France	Session chair (Emerging Memory), TPC member (Emerging Technologies, Systems and Applications)
ISCAS 2013 (IEEE International Symposium on Circuits and Systems)	19th – 23rd May 2013	Beijing, China	Special session organizer (Silicon photonics based on-chip architectures)
DAC 2013 (Design Automation Conference)	2nd-6th June 2013	Austin (TX), USA	TPC member (Emerging Technologies)
NEWCAS 2013 (IEEE International New Circuits and Systems Conference)	16th-19th June 2013	Paris, France	Special session co-organizer (Design methods for emerging technologies), TPC member, Track chair (CAD and Design Tools)
Nanoarch 2013 (IEEE/ACM International Symposium on Nanoscale Architectures)	15th-17th July 2013	New York, NY, USA	TPC member
VLSI-SoC 2013 (IFIP/IEEE International Conference on Very Large Scale Integration)	7th-9th October 2013	Istanbul, Turkey	Session organizer and chair (Nanoscale Logic Fabrics – the Status of Switches) TPC member (Devices, Circuits and Systems for Emerging Technologies)
FETCH 2014 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	8th-10th January 2014	Ottawa, ON, Canada	Steering committee member
DATE 2014 (Design Automation and Test in Europe)	24th-28th March 2014	Dresden, Germany	Executive Committee Member, Special Day Co-Chair (Advancing Electronics Beyond CMOS), Session chair ("Almost There" Emerging Technologies), TPC member
DDECS 2014 (IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems)	23rd-25th April 2014	Warsaw, Poland	Topic Chair
FTFC 2014 (Faible Tension Faible Consommation)	4th-6th May 2014	Monaco	TPC member
ReCoSoC 2014 (International Symposium on Reconfigurable Communication-centric Systems-on-Chip)	26th-28th May 2014	Montpellier, France	Program co-chair, special session chair (Emerging Technologies)
DAC 2014 (Design Automation Conference)	1st-5th June 2014	San Francisco (CA), USA	Member of Outstanding PhD Dissertation Award (OPDA) committee
NEWCAS 2014 (IEEE International New Circuits and Systems Conference)	22nd-25th June 2014	Trois-Rivières (QC), Canada	TPC member (CAD and Design Tools)
PRIME (PhD research in microelectronics and electronics) 2014	30th June – 3rd July 2014	Grenoble, France	TPC member, session chair (Reliability analysis of analog, digital and smart power ICs)
ISVLSI 2014 (IEEE International Symposium on VLSI)	9th-11th July 2014	Tampa, FL, USA	TPC member (Emerging and post-CMOS technologies)
VLSI-SoC 2014 (IFIP/IEEE International Conference on Very Large Scale Integration)	6th-8th October 2014	Playa del Carmen, Mexico	Topic co-chair (3D Integration), Session chair (Memory Architectures & NoC)
ICECS 2014 (IEEE International Conference on Electronics, Circuits, and Systems)	8th-10th December 2014	Marseille, France	Special session organizer and chair (EDA for heterogeneous systems and phenomena), Session chair (Reliability Considerations for Constrained Electronics)
FETCH 2015 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	7th-9th January 2015	Louvain-la-Neuve, Belgium	Steering committee member, Steering Committee Liaison chair
DATE 2015 (Design Automation and Test in Europe)	9th-13th March 2015	Grenoble, France	Topic co-chair (D6: Emerging Technologies and Systems), Session chair (Emerging Technologies for NoC), Session co-chair (Hot Topic – Monolithic 3D: A path to real 3D integrated chips), Panel member (Critical Research Areas Driven By Industry Transformations), Panel moderator (OPTICS workshop)
DAC 2015 (Design Automation Conference)	7th-11th June 2015	San Francisco (CA), USA	TPC member (Emerging Technologies)

Conference Name	*Dates*	*Place*	*Role*
ISVLSI 2015 (IEEE International Symposium on VLSI)	8th-10th July 2015	Montpellier, France	Track chair (Emerging and post-CMOS technologies)
Nanoarch 2015 (IEEE/ACM International Symposium on Nanoscale Architectures)	8th-10th July 2015	Boston, MA, USA	Program chair, Session chair (Concept papers), Awards committee chair
VLSI-SoC 2015 (IFIP/IEEE International Conference on Very Large Scale Integration)	5th-7th October 2015	Daejon, S. Korea	TPC member (System architectures NoC, 3D, multi-core, and reconfigurable)
EJC 2015 (Entretiens Jacques Cartier)	1st-2nd December 2015	Lyon, France	General co-chair
FETCH 2016 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	6th-8th January 2016	Villard-de-Lans, France	Steering committee member
DATE 2016 (Design Automation and Test in Europe)	14th-18th March 2016	Dresden, Germany	Topic co-chair (D6: Emerging Technologies and Systems), Session chair (Hot Topic: In-memory Computing: Status and Trends), Session co-chair (Biochips, Non-volatile Memory Design Methodologies), Panel moderator (OPTICS workshop), Panel member (Will current memories be replaced by new emerging NV memories? When and which ones?)
DAC 2016 (Design Automation Conference)	5th-9th June 2016	Austin (TX), USA	TPC member (Emerging Technologies)
NEWCAS 2016 (IEEE International New Circuits and Systems Conference)	26th-29th June 2016	Vancouver (BC), Canada	Track chair (CAD and Design Tools)
Nanoarch 2016 (IEEE/ACM International Symposium on Nanoscale Architectures)	18th-20th July 2016	Beijing, China	TPC member
MCSoC 2016 (IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip)	21st-23rd September 2016	Lyon, FR	Program Chair, Best Paper Award Committee Chair, Session Chair (Emerging Technologies and Paradigms)
VLSI-SoC 2016 (IFIP/IEEE International Conference on Very Large Scale Integration)	26th-28th September 2016	Tallinn, Estonia	General co-chair, Best Paper Award Committee member, Session chair (Reliability and Design for Test)
FETCH 2017 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	9th-11th January 2017	Mont Tremblant, QC, Canada	Steering committee member
DATE 2017 (Design Automation and Test in Europe)	27th-31st March 2017	Lausanne, Switzerland	Executive Committee Member, Track Chair (Application Design), Member of Best Paper Award committee, Member of Outstanding Dissertation Award (ODA) committee
DAC 2017 (Design Automation Conference)	18th-22th June 2017	Austin (TX), USA	External reviewer
NEWCAS 2017 (IEEE International New Circuits and Systems Conference)	25th-28th June 2017	Strasbourg, France	Session co-chair (Imaging and Sensing Circuits), TPC member (CAD, Device Modeling & Design Tools)
Nanoarch 2017 (IEEE/ACM International Symposium on Nanoscale Architectures)	25th-26th July 2017	Newport, USA	TPC member
VLSI-SoC 2017 (IFIP/IEEE International Conference on Very Large Scale Integration)	23rd-25th September 2017	Abu Dhabi, UAE	Steering Committee member
FETCH 2018 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	24th-26th January 2018	Saint-Malo, France	Steering committee member

Conference Name	*Dates*	*Place*	*Role*
DATE 2018 (Design Automation and Test in Europe)	19th-23rd March 2018	Dresden, Germany	Executive Committee Member, Track Chair (Application Design), Member of Best Paper Award committee, Member of Outstanding Dissertation Award (ODA) committee, Tutorial co-organizer (Emerging Technologies for Computing - from devices to systems), Special session co-organizer (Computing with Ferroelectric FETs – Devices, Models, Systems and Applications), Special Session co-chair (Computing with Emerging Memories: How Good can it be?), Panel Chair (Workshop W02 Emerging Memory Solutions & Applications - Technology, Manufacturing, Architectures, Design, Automation and Test)
ISCAS 2018 (IEEE International Symposium on Circuits and Systems)	27th – 30th May 2018	Florence, Italy	TPC member
DAC 2018 (Design Automation Conference)	24th-28th June 2018	San Francisco (CA), USA	External reviewer
NEWCAS 2018 (IEEE International New Circuits and Systems Conference)	24th-27th June 2018	Montreal (QC), Canada	TPC member (CAD, Device Modeling & Design Tools)
Nanoarch 2018 (IEEE/ACM International Symposium on Nanoscale Architectures)	18th-19th July 2018	Athens, Greece	TPC member
VLSI-SoC 2018 (IFIP/IEEE International Conference on Very Large Scale Integration)	8th-10th October 2018	Verona, Italy	Steering Committee member, Track co-chair (Digital architectures: NoC, multi- and many-core, hybrid, and reconfigurable)
DCIS 2018 (Design of Circuits and Integrated Systems Conference)	21st-23rd November 2018	Lyon, France	General Chair
ICECS 2018 (IEEE International Conference on Electronics, Circuits, and Systems)	9th-12th December 2018	Bordeaux, France	TPC member (Circuit Design: EDA CAD optimization test and reliability)
FETCH 2019 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	28th-30th January 2019	Louvain-la-Neuve, Belgium	Steering committee member
DATE 2019 (Design Automation and Test in Europe)	25th-29th March 2019	Florence, Italy	Executive Committee Member, Track Chair (Application Design), Member of Best Paper Award committee, Member of Outstanding Dissertation Award (ODA) committee, Session chair (Emerging technologies for better NoCs), Special Session co-chair (Rebooting our Computing Models), Panel member (Bringing on-chip optical interconnects into the real world)
DAC 2019 (Design Automation Conference)	2nd-5th June 2019	Las Vegas (NV), USA	External reviewer
NEWCAS 2019 (IEEE International New Circuits and Systems Conference)	23rd-26th June 2019	Munich, Germany	TPC member (CAD & Design Tools)
PRIME (PhD research in microelectronics and electronics) 2019	5th-8th July 2019	Lausanne, Switzerland	TPC member
Nanoarch 2019 (IEEE/ACM International Symposium on Nanoscale Architectures)	17th-19th July 2019	Qingdao, China	TPC member
ISLPED 2019 (ACM/IEEE International Symposium on Low Power Electronics and Design)	29th-31st July 2019	Lausanne, Switzerland	TPC member (Logic and Architecture)
SOCC 2019 (IEEE International System-on-Chip Conference)	3rd-6th September 2019	Singapore	International liaison
VLSI-SoC 2019 (IFIP/IEEE International Conference on Very Large Scale Integration)	6th-9th October 2019	Cuzco, Peru	Steering Committee member, Track chair (Emerging technologies and computing paradigms)
ICECS 2019 (IEEE International Conference on Electronics, Circuits, and Systems)	27th-29th November 2019	Genova, Italy	TPC member (EDA CAD, Test and Reliability)

Conference Name	*Dates*	*Place*	*Role*
FETCH 2020 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	12th-14th February 2020	Montreal, QC, Canada	Steering committee member
DATE 2020 (Design Automation and Test in Europe)	9th-13th March 2020	Grenoble, France (virtual)	Executive Committee Member, Vice-Program Chair, Special Session co-chair (Emerging Neural Algorithms and Their Impact on Hardware), Session chair (Special Day on "Silicon Photonics": High-Speed Silicon Photonics Interconnects for Data Center and HPC), Panel Chair (Workshop on Computing-in-Memory: from Device to Applications)
ISCAS 2020 (IEEE International Symposium on Circuits and Systems)	17th – 20th May 2020	Seville, Spain (virtual)	TPC member
ISLPED 2020 (ACM/IEEE International Symposium on Low Power Electronics and Design)	10th-12th August 2020	Boston, MA, USA (virtual)	TPC member (Logic and Architecture)
VLSI-SoC 2020 (IFIP/IEEE International Conference on Very Large Scale Integration)	5th-7th October 2020	Salt Lake City, USA (virtual)	Steering Committee member, Track chair (Emerging technologies and computing paradigms), Publicity chair
DATE 2021 (Design Automation and Test in Europe)	1st-5th February 2021	Grenoble, France (virtual)	Executive Committee Member, Program Chair, Member of Best Paper Award Committee, Keynote chair (Privacy this unknown - The new design dimension of computing architecture)
VLSI-SoC 2021 (IFIP/IEEE International Conference on Very Large Scale Integration)	5th-7th October 2021	NTU, Singapore	Steering Committee member, Publicity co-chair, TPC member
Nanoarch 2021 (IEEE/ACM International Symposium on Nanoscale Architectures)	8th-10th November 2021	Thrace, Greece	TPC member
DATE 2022 (Design Automation and Test in Europe)	14th-23rd March 2022	Antwerp, Belgium (virtual)	Vice-General Chair, Chair of Ferroelectronics workshop
ETS 2022 (IEEE European Test Symposium)	23rd-27th May 2022	Barcelona, Spain	TPC member
FETCH 2022 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	15th-17th June 2022	Les Houches, France	Steering committee member
DAC 2022 (Design Automation Conference)	10th-14th July 2022	San Francisco (CA), USA	TPC member (Emerging Technologies)
VLSI-SoC 2022 (IFIP/IEEE International Conference on Very Large Scale Integration)	3rd-5th October 2022	Patras, Greece	Steering Committee member
ICRC 2022 (International Conference on Rebooting Computing)	8th-9th December 2022	San Francisco, USA	TPC member, Special Session co-organizer (Logic Synthesis for Low-Temperature Electronics)
Nanoarch 2022 (IEEE/ACM International Symposium on Nanoscale Architectures)	8th-9th December 2022	Virtual	TPC member
FETCH 2023 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	7th-9th February 2023	Lavey-les-Bains, Switzerland	Steering committee member
DATE 2023 (Design Automation and Test in Europe)	17th-19th April 2023	Antwerp, Belgium	General Chair, Focus Session co-organizer (Cross-Layer Design for the Predictive Assessment of Technology-Enabled Architectures)
DAC 2023 (Design Automation Conference)	9th-13th July 2023	San Francisco (CA), USA	TPC member (Emerging Technologies)
VLSI-SoC 2023 (IFIP/IEEE International Conference on Very Large Scale Integration)	16th-18th October 2023	Sharjah, UAE	Steering Committee member, Special Session Chair (Special Session: Advances and challenges in ferroelectric in memories and computing)
FETCH 2024 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	7th-9th February 2024	Maillen, Belgique	Steering committee member

Conference Name	*Dates*	*Place*	*Role*
DATE 2024 (Design Automation and Test in Europe)	25th-27th March 2024	Valencia, Spain	Past General Chair, Focus Session co-organizer and session Chair (Smoothing Disruption Across the Stack: Tales of Memory Technology, Heterogeneity, & Compilers), IEEE CEDA Distinguished Lecturer Lunchtime Keynote session Chair, EDAA Outstanding Dissertation Awards Chair
DAC 2024 (Design Automation Conference)	23rd-27th June 2024	San Francisco (CA), USA	TPC member (Emerging Technologies)
VLSI-SoC 2024 (IFIP/IEEE International Conference on Very Large Scale Integration)	6th-9th October 2024	Tanger, Morocco	Steering Committee member, Track Chair (Design for AI hardware and emerging applications)
ICCAD 2024 (ACM/IEEE International Conference on Computer-Aided Design)	27th-31st October 2024	Newark, NJ, USA	TPC member Track 3.3 Nanoscale and Post-CMOS Systems
FETCH 2025 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	12th-14th February 2025	Montreal, Canada	Steering committee member
DATE 2025 (Design Automation and Test in Europe)	1st-3rd April 2025	Lyon, France	Local Arrangements Chair, Workshop co-General Chair (Cross-stack Explorations of Ferroelectric-based Logic and Memory Solutions for At-Scale Compute Workloads), Panel member (Improving Chip Design Enablement for Universities in Europe), EDAA Outstanding Dissertation Awards Chair
DAC 2025 (Design Automation Conference)	22nd-25th June 2025	San Francisco (CA), USA	TPC Track Chair (Emerging Technologies)
VLSI-SoC 2025 (IFIP/IEEE International Conference on Very Large Scale Integration)	12th-15th October 2025	Puerto Varas, Chile	Steering Committee member
ICCAD 2025 (ACM/IEEE International Conference on Computer-Aided Design)	26th-30th October 2025	Munich, DE	TPC member
FETCH 2026 (Ecole d'hiver francophone sur la technologie de conception de systèmes embarqués hétérogènes)	4th-6th February 2026	Lavey-les-Bains, Suisse	Steering committee member
DATE 2026 (Design Automation and Test in Europe)	20th-22nd April 2026	Verona, Italy	Workshop co-General Chair (W04 Rapid Design Space Explorations of Novel Hardware Solutions: from Atoms to Applications), Session chair (TS03 Routing, Mapping, and Interconnects for Scalable Hardware Systems), EDAA Outstanding Dissertation Awards Chair
ECTC 2026 (IEEE Electronic Components and Technology Conference)	26th-29th May 2026	Orlando, FL, USA	Panel co-organizer and co-chair (AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging)
DAC 2026 (Design Automation Conference)	25th-29th July 2026	Long Beach (CA), USA	TPC Track Chair (Emerging Technologies), Best Paper Award committee member
ICCAD 2026 (ACM/IEEE International Conference on Computer-Aided Design)	8th-12th October 2026	San Jose, CA, USA	TPC member (Track 3.3 Nanoscale and Post-CMOS Systems)
VLSI-SoC 2026 (IFIP/IEEE International Conference on Very Large Scale Integration)	11th-14th October 2026	Limassol, Cyprus	General co-Chair, Steering Committee member
ICECS 2026 (IEEE International Conference on Electronics, Circuits, and Systems)	8th-11th November, 2026	Thessaloniki, Greece	TPC member (Technology)
DATE 2027 (Design Automation and Test in Europe)	22nd-24th April 2027	Dresden Germany	Date Sponsors Committee Chair
DAC 2027 (Design Automation Conference)	11th-14th July 2027	San Jose (CA), USA	TPC Track Chair (Emerging Technologies)

Supervision and training activities[1]

MSc students

Name	*Nature of degree*	*Period*	*Funding*	*% co-supervision*	*Title of thesis*
L. Andraud	MSc Integrated Electronic Devices, ECL	April - September 2001	CNRS/ECL	100%	Développement en Java d'une plate forme CAO pour systèmes analogiques haute fréquence (*Development of a Java CAD platform for high-frequency analog systems*)
M. Brière	MSc Integrated Electronic Devices, UCB Lyon	January-September 2002	CNRS/ECL	50% with F. Gaffiot	Modélisation comportementale d'un détecteur de fluorescence (*Behavioral modeling of a fluorescence-based biomolecule detector*)
F. Castro Alves Filho	MSc Electronic Engineering, U. Campinas, BR	March-September 2002	CNRS/ECL	100%	Méthodologies de conception de circuits à très haut débit de télécommunications à base de HBT (*Design methodologies for high frequency telecommunication circuits using HBT*)
T. Michalke	MSc Electronic Engineering, TU Darmstadt, DE	March-September 2003	ACI Nanosciences	50% with F. Mieyeville	Modèles comportementaux pour la simulation de réseaux optiques intégrés reconfigurables en longueur d'onde (*Behavioral models for the simulation of on-chip wavelength-reconfigurable networks*)
P. Lisik	MSc Electronic Engineering, TU Lodz, PL	April-September 2003	Polonium	100%	Optimization algorithms for analog EDA
M. Owczarek	MSc Electronic Engineering, TU Lodz, PL	April-September 2003	Polonium	100%	Graphical user interface for analog EDA tool
R. Bonnet	MSc Engineering, ECAM	March-September 2004	Région Rhône-Alpes	50% with F. Mieyeville	Etude, modélisation et conception de la partie RF d'un central d'information automobile embarqué (*Analysis, modeling and design of RF blocks in an automotive information system*)
H. Nguyen Huu	MSc Engineering, ECL	April-September 2004	Région Rhône-Alpes	100%	Méthodes hiérarchiques de conception de SoCs extrêmement hétérogènes (*Hierarchical design methods for extremely heterogeneous SoC)*
E. Mastreani	MSc Integrated Electronic Devices, INSA Lyon	January - September 2005	Région Rhône-Alpes	50% with L. Quiquerez	Dimensionnement automatique de microsystèmes biomédicaux (*Automated sizing of biomedical microsystems*)
R. Du	MSc Integrated Electronic Devices, ECL	April – September 2005	SNECMA	100%	Méthodes de conception de microsystème pour l'aéronautique (*Design methods for aeronautical microsystems*)
G. Revy	MSc Computer Science, UT Belfort-Montbéliard	April – September 2005	Région Rhône-Alpes	100%	Interfaces pour l'optimization hiérarchique de systèmes hétérogènes (*Interfaces for hierarchical optimization of heterogeneous systems*)
X. Yang	MSc Integrated Electronic Devices, ECL	January - September 2007	ANR^{PNANO}	50% with I. Hassoune	Architectures d'additionneur 16-bit à base de DGMOS à grilles asymétriques (*16-bit asymmetric DGMOS-based adder architectures*)
N. Darbinyan	MSc Business Administration, Université Lyon 3	March - September 2007	Nano2008	100%	Modélisation de méthodes de conception pour systèmes sur puce hétérogènes (*Design process modeling for heterogeneous systems on chip*)
P.E. Gaillardon	MSc Integrated Electronic Devices, INSA Lyon	April - September 2008	CPE	50% with R. Daviot	Architectures logiques à base de portes reconfigurables nanoélectroniques (*Logic architectures using reconfigurable nanoelectronic gates*)
P. Piotrow	MSc Electronic Engineering, TU Lodz, PL	April-September 2009	Polonium	100%	Reconfigurable nanocell matrices and functions
W. Zajączkowski	MSc Electronic Engineering, TU Lodz, PL	April-August 2010	ANR^{ARPEGE} Nanograin	100%	3D Single Electron Memory Architecture

[1] The percentages in the tables indicate my amount of participation in the role of supervision and training: definition and orientation of topics and objectives, day-to-day supervision and verification of final results, manuscripts and publications.

T. Cretinon	MSc Electronic and Computer Engineering, CPE	March-July 2011	CATRENE 3DIM3	20% with L. Labrak	Information structuring for heterogeneous 3DIC design exploration and partitioning
M. Rozak	MSc Electronics Engineering, TU Lodz, PL	September -December 2015	Erasmus	100%	Dynamic body biasing in advanced transistors
Y. Megna	MSc Embedded Systems Electronics, Lyon	April-October 2017	ANR$^{\text{Générique}}$ HELICITY	50%	Predictive modeling of complex systems
M. Cantan	MSc Embedded Systems Electronics, Lyon	April-October 2018	ANR$^{\text{Générique}}$ HELICITY	100%	Energy-efficient edge computing with integrated ferroelectric devices
S. Bouchra	MSc Embedded Systems Electronics, Lyon	April-October 2019	ANR$^{\text{Générique}}$ LEGO	100%	Optimization of sensor hub board configuration
L. Mozzone	MSc Electronics Engineering, Politecnico di Torino, IT	September 2019-January 2020	H2020-ICT 3εFerro	50%	Ferroelectric logic in memory architectures
C. Maclean	MSc Nanoscale Engineering, University of Lyon	April-September 2020	ANR$^{\text{Générique}}$ LEGO	100%	Logic Circuit Design with Vertical Nanowire Field Effect Transistors
H. Maitre	MSc CPE Lyon	June-November 2022	ANR$^{\text{Générique}}$ LEGO	100%	Development of optimized VNWFET-based logic cell library
S. Saoudi	MSc Ecole Polytechnique Tunisie, TN	April-September 2023	ANR$^{\text{Générique}}$ Octane	100%	System-level integration and assessment of photonic computing accelerator
G. Loubet	MSc Embedded Systems Electronics, Lyon	March-September 2025	H2020-ICT FVLLMONTI	100%	Reliability study of a 3D embedded AI compute cube based on vertical nanowire devices
P. Sakey Shamu	MSc Nanoscale Engineering, University of Lyon	April-September 2026	PEPR-Electronique FerroFutures	50%	Design–Technology Co-Optimization of Ferroelectric Memristive Capacitance (MemCap) Devices and Crossbar-Based MAC Circuits for Neuromorphic Computing
V. Martin	MSc Embedded Systems Electronics, Lyon	March-September 2026	PEPR-Electronique CHOOSE	100%	Peripheral circuitry evaluation and design for Analog in-Memory-Computing

PhD students

Name	*Nature of degree*	*Period*	*Funding / Scholarship*	*% co-supervision*	*Title of thesis*
F. Mieyeville	PhD Integrated Electronic Devices, ECL. Defended on 30 October 2001.	September 1998 – October 2001	MENRT	30% with F. Gaffiot and G. Jacquemod, principal advisors	Modélisation de liaisons optiques inter- et intra-puces à haut-débit (*Modeling of high data rate inter- and intra-chip links*)
G. Tosik	PhD Integrated Electronic Devices, ECL. Defended on 28 January 2004.	September 2000 – September 2003	MENRT	50% with F. Gaffiot, principal advisor	Conception et modélisation de la répartition de l'horloge des systèmes intégrés par voie optique (*Design and modeling of integrated optical clock distribution systems*)
F. Tissafi-Drissi	PhD Integrated Electronic Devices, ECL. Defended on 13 December 2004.	September 2001 – December 2004	MENRT	75% with F. Gaffiot, principal advisor	Méthodes et outils de synthèse pour systèmes multi-domaine (*Synthesis methods and tools for multi-domain systems*)
M. Brière	PhD Integrated Electronic Devices, ECL. Defended on 29	September 2002 – September	MENRT	50% with F. Gaffiot, principal	Réseaux sur puce reconfigurables en longueur d'onde (*Wavelength-reconfigurable networks on chip*)

	November 2005.	2005		advisor	
S. Dia	PhD Integrated Electronic Devices, ECL. Defended on 19 December 2006.	October 2003 – October 2006	Région Rhône-Alpes	Principal advisor; 45% with F. Gaffiot and F. Mieyeville	Outils de conception de blocs radiofréquences et optiques dans les systèmes sur puce (*Design tools for RF and optical blocks in systems on chip*)
J. Liu	PhD Integrated Electronic Devices, ECL. Defended on 19 November 2008.	October 2005 – September 2008	MENRT	Principal advisor; 90% with F. Gaffiot	Architectures reconfigurables à base de CNTFET double grille (*Double-gate CNTFET-based reconfigurable architectures*)
M. Owczarek	PhD Electronic Engineering, TU Lodz. Defended on 2 March 2018.	January 2005 – December 2009	TU Lodz scholarship	30% with F. Gaffiot and Z. Lisik, principal advisor	Design and optimization of photonic systems
H. Filiol	PhD Integrated Electronic Devices, ECL. Defended on 22 July 2010.	October 2006 - September 2009	BDI CNRS / CEA	Principal advisor; 50% with D. Morche	Architectures analogiques adaptées aux technologies nanométriques et méthodes de conception associées (*Nanometer technology based analog architectures and associated design methods*)
Y. Felk	PhD Economy - Organization - Society, Mines ParisTech. Defended on 11 February 2011.	November 2007 – November 2010	CIFRE (STMicroelectronics)	10% with P. Masson, B. Weil, principal advisor	Evaluation et pilotage des activités de recherche dans la R&D centrale de STMicroelectronics - Nouveaux principes de management de la recherche industrielle pour l'innovation de rupture
W. Du	PhD Integrated Electronic Devices, ECL. Defended on 14 September 2011.	September 2008 – September 2011	MENRT	Principal advisor; 10% with F. Mieyeville, D. Navarro	Modélisation et simulation de réseaux de capteurs sans fil (*Modeling and simulation of wireless sensor networks)*
P.E. Gaillardon	PhD Integrated Electronic Devices, ECL. Defended on 15 September 2011.	September 2008 – September 2011	CEA	Principal advisor; 50% with F. Clermidy	Architectures de calcul reconfigurables et à base de composants moléculaires (*Reconfigurable computing architectures based on molecular devices)*
	*** **Recipient of Best Centrale Innovation Thesis Award** ***				
V. Viswanathan	PhD Integrated Electronic Devices, ECL. Defended on 6 September 2012.	October 2009 – October 2012	ANR^{PNANO} 3D-IDEAS	Principal advisor; 50% with D. Navarro	Modeling and design of 3D imager ICs
K. Jabeur	PhD Integrated Electronic Devices, ECL. Defended on 11 September 2012.	September 2009 – September 2012	ANR^{ARPEGE} Nanograin	Principal advisor; 70% with S. Le Beux	Ambipolar Independent Double Gate FET (Am-IDGFET) logic design - Methods and Techniques
F. Frantz	PhD Integrated Electronic Devices, ECL. Defended on 26 October 2012.	September 2009 – September 2012	CATRENE 3DIM3	Principal advisor; 100%	Architectural exploration methods and tools for heterogeneous 3D-IC
M. Galos	PhD Integrated Electronic Devices, ECL. Defended on 15 November 2012.	October 2009 – October 2012	MENRT	Principal advisor; 10% with F. Mieyeville, D. Navarro	Reconfiguration dynamique et simulation fine modélisée au niveau transaction dans les réseaux de capteurs sans fil hétérogènes matériellement / logiciellement (*Hardware/software heterogeneity in wireless sensor networks: Dynamic reconfiguration and accurate transaction-level modeling*)
N. Zhu	PhD Integrated Electronic Devices, ECL. Defended on 11 October 2013.	September 2010 – September 2013	Chinese Scolarship Council	Principal advisor; 100%	Simulation and Optimization of Energy Consumption on Wireless Sensor Networks
Z. Feng	PhD Integrated Electronic Devices, ECL. Defended on 31 January 2014.	September 2010 – September 2013	Chinese Scolarship Council	Principal advisor; 10% with D. Navarro	High-level design and simulation of CMOS Image Sensors
Z. Li	PhD Integrated	October	MENRT	Principal	Architectures de calcul exploitant les spécificités

	Electronic Devices, ECL. Defended on 28 January 2015.	2011 – October 2014		advisor; 30% with S. Le Beux, C. Monat	de l'optique non-linéaire (*Computing architectures based on non-linear optics*)
R. Cao	PhD Integrated Electronic Devices, ECL. Defended on 25 March 2016.	January 2013- January 2016	CIFRE Mentor Graphics	Principal advisor; 30% with A. Arriordaz	DRC and LVS for Silicon Photonics
H. Li	PhD Integrated Electronic Devices, ECL. Defended on 9 December 2016.	October 2013 – October 2016	Chinese Scolarship Council	Principal advisor; 30% with S. Le Beux	Toward an efficient interface for optical network on chip
O. Dubray	PhD Integrated Electronic Devices, ECL. Defended on 2 February 2017.	October 2013 – October 2016	CEA-LETI	Principal advisor; 30% with S. Menezo	Conception, Fabrication et Test d'un Emetteur/Récepteur électro-optique de capacité 1Tb/s pour les transmissions courtes distances (*Design, fabrication and test of a 1Tb/s electro-optical transceiver for short-distance communications*)
A. Perodou	PhD Control Engineering. Defended on 18 December 2019.	May 2016 – May 2019	Région Rhône-Alpes	Principal advisor; 30% with G. Scorletti, A. Korniienko	Frequency Design of Passive Electronic Filters: a Modern System Approach
S. Rigault	PhD Integrated Electronic Devices, ECL. Defended on 8 December 2020.	February 2017 – February 2020	CIFRE STMicro-electronics	Principal advisor; 30% with L. Labrak, N. Moeneclaey	Study and Design of a Low-Voltage and Power-Efficient Sub-ns Pulse Integrated CMOS VCSEL Driver for SPAD-based Direct Time-of-Flight Rangefinding in Consumer Mobile Electronics
A. Brik	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 21 September 2021.	September 2017 – September 2020	ANR$^{\text{Générique}}$ HELICITY	Principal advisor; 50% with L. Labrak	Design methods for integrated multi-physics and continuous-discrete systems
M. Cantan	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 5 July 2023.	October 2018 – December 2022	H2020-ICT-3εFerro	Principal advisor; 40% with C. Marchand, D. Deleruyelle	Energy-efficient edge computing with ferroelectric devices
A. Poittevin	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 23 June 2022.	December 2018 – December 2021	ANR$^{\text{Générique}}$ LEGO	Principal advisor; 40% with S. Le Beux, C. Marchand	Logic circuits based on vertical nanowire FETs: Physical and circuit design challenges and opportunities
C. Zrounba	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 11 December 2023.	January 2019 – May 2023	ANR$^{\text{Générique}}$ OpticALL^2	Principal advisor; 40% with S. Le Beux, F. Pavanello	Modeling integrated photonic devices based on phase-change materials
E. Dupuis	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 10 May 2022.	April 2019 – April 2022	ANR$^{\text{Générique}}$ AdequatDL	Co-advisor; 50% with A. Bosio	Weight-sharing methods for retraining-free CNN compression
M.S. Abdalla	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 16 December 2024.	March 2021 – June 2024	ECLAusion	Principal advisor, 30%; with F. Pavanello, C. Marchand	Neuromorphic computing in Lithium Niobate on Insulator platforms
A. Piri	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended on 17 December 2024.	September 2021 – September 2024	H2020-MSC-APROPOS	Co-advisor; 50% with A. Bosio	Design space exploration for accuracy-aware computing
R. Cardoso	PhD Electronics, Micronanoelectronics,	October 2021 –	ANR$^{\text{Générique}}$ Octane	Principal advisor; 50%	Dynamic Matrix Multiplications in Memory with Photonics and Phase-Change Materials

	Optics and Lasers, ECL. Defended on 10 October 2024.	October 2024		with S. Le Beux	
S. Mannaa	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended in 2025	October 2022 – October 2025	H2020-ICT-FVLLMONTI	Principal advisor; 50% with A. Bosio	3D embedded AI compute cube based on vertical nanowire devices
M. Vidaletti Costa	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defended in 2026	February 2023 – February 2026	H2020-REDI	Principal advisor; 50% with A. Mitchell	Large-scale photonic CNNs integrated on-chip based on Lithium Niobate on Insulator (LNOI) platforms
L. Rhétat	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defense expected in January 2027	January 2024 – January 2027	CEA Grenoble	Principal advisor; 30% with J.P. Noel	Study and design of secure memory circuits based on FeRAM technology
H. Benamara	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defense expected in February 2027	February 2024 – February 2027	PEPR Electronique / AC CHOOSE	Principal advisor; 30% with M. Kooli, P. Vivet	Methodology for system-technology co-optimization of near-memory computing architectures
R. Pronsato	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defense expected in March 2027	March 2024 – March 2027	PEPR Electronique / AC CHOOSE	Principal advisor; 70% with P. Vivet	Emerging Design-Technology Co-Optimization Methodologies
A. Cauquil	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defense expected in September 2027	September 2024 – September 2027	Horizon Europe – Ferro4EdgeAI	Principal advisor; 50% with D. Deleruyelle	In-Memory-Computing Accelerator Design and Benchmarking based on Next-Generation Ferroelectric Technology
L. Martin Wisniewski	PhD Engineering Sciences, Micro- and Nanoelectronics, Aix-Marseille University. Defense expected in October 2027	October 2024 – October 2027	PEPR Electronique / PC FerroFutures	Co-advisor; 30% with J.M. Portal, F. Melul	Design of FeRAM technology test vehicles for in-memory computing applied to neural networks
M. Remillieux	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defense expected in September 2028	October 2025 – October 2028	PEPR IA / PC Adapting	Principal advisor; 50% with D. Chillet	Optical interconnects for efficient and flexible AI hardware accelerators
A. Laradji	PhD Electronics, Micronanoelectronics, Optics and Lasers, ECL. Defense expected in September 2029	September 2026 – September 2029	CIFRE STMicro-electronics	Principal advisor; 30% with L. Labrak, F. Abouzeid	Robust and efficient co-design methodology for interconnected chiplets and their packaging for space and defense applications

Research engineers

Name	*Period*	*Funding*	*% co-*	*Topic*

			supervision	
F. Teysseyre	September 2013 – August 2015	CATRENE H-Inception	50% with D. Navarro	High-level modeling techniques for optical path and optical image sensors in SystemC-MDVP

Postdoctoral research associates

Name	*Period*	*Funding*	*% co-supervision*	*Topic*
E. Drouard	September 2003 – August 2004	CNRS-STIC	50% with X. Letartre	Reconfigurable photonic networks for optical interconnections in microelectronics
F. Tissafi-Drissi	January 2005 – December 2005	FP6-IST-PICMOS	100%	Models and design methods for integrated optical interconnect
I. Hassoune	June 2006 - July 2007	ANR^{PNANO} Multigrilles	50% with D. Navarro	Design of novel logic cells based on double-gate MOSFETs
S. Burignat	September 2006 - August 2007	CNRS-ST2I	100%	Exploration of nanosystem architectures
H. Charlery	March 2007 - January 2008	Nano2008 / STMicroelectronics	100%	Predictive design methods for heterogeneous systems on chip
A. Allam	October 2008- September 2010	FP7-ICT-WADIMOS	100%	Optical interconnect for Multiprocessor SoC
L. Labrak	January 2009- December 2012	Nano2013 / STMicroelectronics, FP7-ICT-HELIOS	100%	Predictive design for heterogeneous 3D ICs
B. Wang	April 2009- October 2010	FP7-ICT-HELIOS	50% with E. Drouard	Modeling and design methods for Photonics on CMOS
N. Yakymets	June 2009- January 2012	ANR^{ARPEGE} Nanograin	70% with S. Le Beux	Nanoreconfigurable circuit design technology
K. Cheng	September 2012-August 2014	LST Grilles-CMOS, ATER ECL	50% with S. Le Beux	Nanoreconfigurable circuit design technology
M. Flores Sepulveda	October 2014- September 2015	LabEx Cominlabs / 3DCORE	30% with S. Le Beux	High-level simulation and design of 3D optical networks on chip
S. Mannaa	November 2025- October 2027	PEPR-Electronique / FerroFutures	100%	DTCO methods and tools for design-space exploration of ferroelectric computing circuits

Participation in examination boards

PhDs

Name	*Date*	*University / Principal advisor*	*Role*	*Title of thesis*
D. Navarro	17th October 2003	Université Montpellier II / Prof. G. Cambon	Examiner	Architecture et conception de rétines silicium CMOS: Application à la mesure du flot optique
S. Riso	28th November 2005	Université de Montpellier II / Prof. M. Robert	Reviewer	Evaluation des paramètres architecturaux des réseaux sur puce
A. Andriahantenaina	16th December 2005	Université de Paris VI / Prof. A. Greiner	Reviewer	Implémentation matérielle d'un micro-réseau SPIN à 32 ports
O. Tintori	15th December 2006	Université de Provence, Aix-Marseille I / Prof. J.L. Autran	Reviewer	Modélisation et simulation des transistors Double-Grille; du dispositif au circuit intégré
N. Lhostis	20th June 2007	Ecole Nationale Supérieure de Télécommunications de Paris / Prof. A. Amara	Reviewer	Techniques et méthodes de conception basse consommation en technologie SOI
M. Oyamada	23rd October 2007	Institut National Polytechnique de Grenoble / A. Jerraya	Reviewer	Estimation de performance du logiciel en systèmes multiprocesseur monopuces
A. Zenati	26th October 2007	Université Joseph Fourier, Grenoble / Prof. S. Basrour	Reviewer	Modélisation et simulation de microsystèmes multi domaines à signaux mixtes : vers le prototypage virtuel d'un microsystème autonome
T. Levi	4th December 2007	Université Bordeaux I / Prof. P. Fouillat	Reviewer	Méthodologie de développement d'une bibliothèque d'IP-AMS en vue de la conception automatisée de systèmes sur puces analogiques et mixtes
A. Tournier	18th December 2007	Université Lyon I / Prof. G.N. Lu	Chairman	Pixel 1-Transistor à modulation de charges pour capteurs d'images CMOS à haute résolution
N. Bruchon	19th December 2007	Université Montpellier II / Prof. L. Torres	Reviewer	Evaluation, validation and design of hybrid CMOS – non-volatile emerging technology cells for dynamically reconfigurable fine grain architecture
Y. Joannon	11th April 2008	Institut Polytechnique de Grenoble / Prof. S. Tedjini	Reviewer	Qualification et génération automatique de stimuli pour le test de systèmes sur puces (SoC) analogiques mixtes et RF
J. Cornet	25th April 2008	Institut Polytechnique de Grenoble / Prof. F. Maraninchi	Examiner	Separation of Functional and Non-Functional Aspects in Transactional Level Models of Systems-on-Chip
W. Heirman	30th May 2008	Universiteit Gent / Prof. J. Van Campenhout	Reviewer	Reconfigurable optical interconnection networks for shared-memory multiprocessor architectures
Y. Layouni	10th July 2008	INSA Lyon / Prof. N. Abouchi	Chairman	Synthèse architecturale de convertisseurs sigma-delta
B. Zongo	3rd September 2008	Institut Polytechnique de Grenoble / Prof. J.M. Fournier	Reviewer	Méthodologie de conception analogique appliquée à un régulateur de tension à faible chute de tension (LDO)
B. Nicolle	11th September 2008	Université de Nice-Sophia Antipolis / Prof. G. Jacquemod	Examiner	Optimization et validation de spécifications pour transmetteurs multi-standards
G. Terrasson	24th November 2008	Université de Bordeaux I / Prof. S. Basrour	Examiner	Contribution a la conception d'un émetteur-récepteur pour microcapteurs autonomes
A. Lewicki	1st December 2008	Université de Nice-Sophia Antipolis / Prof. G. Jacquemod	Reviewer	Conception de modèles haut-niveau pour l'optimization et la vérification de systèmes Bluetooth
X. Loussier	12th December 2008	Université de Provence (Aix-Marseille I) / Dr. D. Munteanu	Chairman	Modélisation et simulation analytique et numérique des nano-transistors multi-grille: du dispositif au circuit intégré

B. Dubois	3rd July 2009	Université de Strasbourg / Prof. F. Braun	Reviewer	Méthodologie de conception de magnétomètre dans une approche mécatronique
O. Leman	11th September 2009	Université de Montpellier II / Prof. P. Nouet	Reviewer	Modélisation et conception d'interfaces faible bruit pour capteurs thermiques micro-usinés: application aux accéléromètres convectifs
J. Goguet	30th September 2009	Université de Bordeaux I / Prof. T. Zimmer	Reviewer	Modélisation compacte du transistor à nanotube de carbone à double grille
S. Jovanovic	6th November 2009	Université de Nancy I / Prof. S. Weber	Reviewer	Architecture reconfigurable de système embarqué auto-organizé
Z. Wang	12th November 2009	Institut Polytechnique de Grenoble / Prof. D. Houzet	Chairman	Design and Multi-Technology Multi-objective Comparative Analysis of Families of MPSOC
F. Guigues	1st December 2009	Université de Provence Sud Toulon Var / Prof. H. Barthélemy	Reviewer	Conception de structures analogiques 'nanowatt' en technologie CMOS standard
C. D'Agostino	8th December 2009	Institut Polytechnique de Grenoble / Dr. Marc Belleville	Reviewer	Estimation statistique de la consommation statique des circuits numériques CMOS
F. Chan Wai Po	23rd July 2010	Université de Bordeaux I / Prof. E. Kerhervé	Reviewer	Conception d'une têt radiofréquence auto adaptative au milieu de propagation pour les applications médicales
K. Alsayeg	1st September 2010	Grenoble INP / Dr. Laurent Fesquet	Chairman	Synthèse de contrôleurs séquentiels QDI faible consommation prouvés corrects
C. Rusu	10th September 2010	Grenoble INP / Prof. M. Nicolaidis	Reviewer	Multi-level fault-tolerance in Networks on Chip
A. Suissa	23rd September 2010	Université Paris VI / Prof. P. Garda	Reviewer	Estimation et optimization de la consommation des systèmes hétérogènes
A. Lecointre	1st October 2010	INSA Toulouse / Prof. R. Plana	Reviewer	Interface radio IR-UWB reconfigurable pour les réseaux de microsystèmes communicants
F. Schwartz	18th November 2010	Université de Strasbourg / Dr. Y. Hervé	Reviewer	Méthodologie de conception d'un système analogique massivement parallèle
T. Mähne	21st February 2011	EPFL / Prof. Y. Leblebici	Reviewer	Efficient Modeling and Simulation Methodology for the Design of Mixed-Signal Systems on Chip
Y.S. Liao	29th April 2011	Université de Bordeaux I / Dr. Cristell Maneux	Reviewer	Caractérisation électrique et électro-optique de transistor à base de nanotube de carbone en vue de leur modélisation compacte"
W. Lafi	11th July 2011	Université de Grenoble / Dr. Ahmed Jerraya	Reviewer	Architectures multiprocesseurs pour applications de télécommunication basées sur les technologies d'intégration 3D
L. Gerrer	12th July 2011	Université de Grenoble / Prof. G. Ghibaudo	Chairman	Impact du Claquage progressif de l'oxyde sur le fonctionnement des composants et circuits MOS : Caractérisation et modélisation.
L. Alves da Silva	16th November 2011	Université de Nice Sophia Antipolis / Prof. G. Jacquemod	Reviewer	Estimation de la consommation d'énergie et du taux d'erreur bit d'un système Bluetooth LE basée sur la modélisation hiérarchique d'un amplificateur de puissance à 2,4 GHz
C. Teodorov	28th November 2011	Université de Bretagne Occidentale / Prof. B. Pottier	Reviewer	Model-driven physical design for future nanoscale architectures
A. Korniienko	6th December 2011	Ecole Centrale de Lyon / Prof. G. Scorletti	Chairman	Réseaux de PLLs distribuées pour synthèse automatique de MPSoCs synchrones
Y. Guillemenet	8th December 2011	Université de Montpellier II / Prof. L. Torres	Reviewer	Logique magnétique pour l'exploration d'architectures reconfigurables
A. Massouri	16th January 2012	Université de Lille I / Dr. A. Kaiser	Chairman	Modélisation comportementale SystemC-AMS d'interfaces RF et liaisons radio multipoints pour réseaux de capteurs
D. Chabi	9th March	Université Paris Sud	Reviewer	Architectures de circuits nanoélectroniques neuro-inspirées

	2012	11 / Prof. J.O. Klein		
A. Porcher	3rd May 2012	Grenoble INP / Dr. Laurent Fesquet	Chairman	Synthèse de circuits asynchrones
G. Abbas	27th June 2012	INSA Lyon / Prof. N. Abouchi	Chairman	Analysis, Modeling, Design and Implementation of Digital Fast-Response Controllers for High-Frequency Low-Power Switching Converters
M. Vasilevski	4th October 2012	Université Paris VI / Dr. H. Aboushady	Chairman	Environnement de conception multi-niveaux unifié appliqué aux systèmes mixtes
J. Dura	18th October 2012	Université Aix-Marseille / Dr. D. Munteanu	Chairman	Modélisation compacte du transport quasi-balistique et quantique pour la simulation des circuits à base de nanofils semi-conducteur en architecture multi-grilles
F. Paugnat	25th October 2012	Grenoble INP / Dr. Laurent Fesquet	Reviewer	Méthode de modélisation et raffinement pour les systèmes hétérogènes
J.C. Krencker	23rd November 2012	Université de Strasbourg / Prof. L. Hébrard	Chairman	Développement d'outils et de modèles CAO de haut niveau pour la simulation électrothermique de circuits mixtes en technologie 3D
C. Killian	5th December 2012	Université de Lorraine / Dr. C. Tanougast	Reviewer	Réseau embarqué sur puce reconfigurable dynamiquement et sûr de fonctionnement
V. Pesca	11th January 2013	Grenoble INP / Prof. L. Anghel	Chairman	Développement des Architectures HW/SW Tolérantes aux Fautes et Auto-calibrantes pour les Technologies Intégrés 3D
A. Samir	21st January 2013	Aix-Marseille Université / Prof. H. Barthélémy	Examiner	Conception de solutions basses puissances et optimization de la gestion d'énergie de circuits dédiés aux applications mixtes
V. Dwarakanath	12th February 2013	Université de Rennes 1 / Prof. O. Sentieys	Chairman	Ultra-Low Power Reconfigurable Architectures for Controllers in Wireless Sensor Network Nodes
M. Jabbar	21st March 2013	Université de Grenoble / Prof. D. Houzet	Reviewer, Chairman	Méthodologies de Conception ASIC Pour des Systèmes sur Puce 3D Hétérogènes à Base de Réseaux sur Puce 3D
A. Joubert	26th March 2013	Université de Grenoble / Dr. D. David	Reviewer	Neurone analogique robuste et technologies émergentes pour les architectures neuromorphiques
S. Bobba	28th May 2013	EPFL / Prof. G. De Micheli	External reviewer	Design methodologies and CAD for emerging nanotechnologies
K. Hamwi	30th May 2013	ENSTA ParisTech / Dr. O. Hammami	Reviewer	Low Power Design Methodology and Photonics Networks on Chip for Multiprocessor System on Chip
D. Soussan	5th July 2013	Université de Grenoble / Dr. M. Belleville	Examiner	Contributions aux Interfaces d'Entrées/Sorties rapides en technologies Silicium-Sur-Isolant partiellement et totalement désertées
H. Cai	9th September 2013	Télécom ParisTech / Dr. J.F. Naviner	Reviewer	Fiabilisation de convertisseurs analogique-numérique à modulation sigma-delta
S. Houssany	13th September 2013	Université de Grenoble / Prof. R. Leveugle	Chairman	Méthodologie d'évaluation de la sensibilité des microprocesseurs vis-à-vis des rayonnements cosmiques
S. Onkaraiah	18th November 2013	Université Aix-Marseille / Prof. C. Muller	Chairman	Modélisation et conception de circuits à base de mémoires non-volatiles résistives innovantes
G. Pollissard	25th November 2013	Université Catholique de Louvain / Prof. D. Flandre	External reviewer	Design techniques for sub-microwatt analog sensor interfaces in advanced CMOS technologies
G. Palma	29th November 2013	Université de Grenoble / Prof. A. Amara	Examiner	Nouvelles Architectures Hybrides: Logique / Mémoires Non-Volatiles et technologies associées
M. Bahmani	9th December 2013	Université de Grenoble / Prof. F. Pétrot	Reviewer	Exploration architecturale et etude des performances des réseaux sur puce 3D partiellement connectés verticalement
H. Ayari	12th December 2013	Université Montpellier 2 / Dr. S. Bernard	Reviewer	Test indirect des circuits analogiques et RF: Contribution pour une meilleure précision et robustesse
L. Bousquet	29th January 2014	Université de Grenoble / Prof. E. Simeu	Reviewer	Génération de modèles de haut niveau enrichis pour les systèmes hétérogènes et multiphysiques
Hraziia	24th February 2014	Télécom ParisTech / Prof. A. Amara	Chairman	Mémoires Embarquées SRAM Non-Volatiles pour la Sauvegarde de l'Information
Z. Cherif	8th April 2014	Télécom ParisTech / Dr. L. Bossuet, Prof. J.L.	Reviewer	Modélisation et caractérisation des fonctions physiquement non-clonables

		Danger		
F. Dupont	19th June 2014	Université de Grenoble / Dr. M. Belleville	Examiner	Intégration de la mesure d'impédance dans un système de stimulation électrique implantable multi-applications: proposition d'une nouvelle stratégie de stimulation
Y. Zhang	11th July 2014	Université Paris Sud / Dr. D. Ravelosona	Reviewer	Modélisation compacte et conception de circuit hybride pour les dispositifs spintroniques basés sur la commutation induite par le courant
T. Cabaret	9th September 2014	Université Paris Sud / Prof. J.O. Klein	Reviewer	Etude, réalisation et caractérisation de memristors organiques électro-greffés en tant que nanosynapses de circuits neuro-inspirés
G. Lecerf	29th September 2014	Université de Bordeaux / Dr. S. Saighi	Reviewer	Développement d'un Réseau de Neurones Impulsionnels sur Silicium à Synapses Memristives
Y. Fkih	14th November 2014	Université Montpellier 2 / Prof. B. Rouzeyre, Dr. M.L. Flottes	Reviewer	Conception en vue du test des circuits intégrés 3D à base de TSVs
O. Ramos	17th November 2014	Université de Nice Sophia Antipolis / Prof. G. Jacquemod	Reviewer	Modélisation et Conception d'un Récepteur Non Cohérent Ultra Large Bande pour les Communications ULB Impulsionnelles dans la Bande de Fréquence 3-5 GHz
C. Metzler	24th November 2014	Université Montpellier 2 / Prof. P. Girard	Reviewer	Test, Reliability and Performance Analysis of TSVs in 3D IC
O. Turkyilmaz	28th November 2014	Université de Grenoble / Prof. R. Leveugle	Reviewer	Emerging 3D technologies for efficient implementation of FPGAs
R. Brum	12th December 2014	Université Montpellier 2 / Prof. L. Torres	Reviewer	Conception hybride CMOS et mémoires magnétiques: applications aux architectures programmables
K. C. Akyel	17th December 2014	Université de Grenoble / Dr. G. Ghibaudo	Chairman	Statistical Methodologies for Modeling the Impact of Process Variability in Ultra-Deep-Submicron SRAMs
N. Bohrer	30th January 2015	Université de Grenoble / Dr. V. Beroulle	Reviewer	Evaluation et amélioration de la sécurité des circuits intégrés analogiques
J. M. Moreno	6th March 2015	TU Wien, Austria / Prof. C. Grimm	External reviewer	Energy Profiling of Networked Embedded Systems
Y. Li	17th June 2015	Université Paris 6 / Dr. M.M. Louërat	Reviewer	Extending SystemC-AMS standard to modeling, design and verification of mixed-signal systems
O. Alcantara	9th September 2015	Université Jean Monnet St Etienne / Prof. F. Rousseau	Reviewer	Synthèse de plateformes d'émulation et évaluation de NoCs pour les systèmes embarqués : vers les réseaux du futur
R. Fei	13th October 2015	Université de Grenoble Alpes / Dr. S. Mir	Chairman	Solutions alternatives pour améliorer le test de production des capteurs optiques en technologie CMOS
Z. Wang	14th October 2015	Université Paris Sud / Prof. J.O. Klein	Chairman	Compact modeling and circuit design based on ferroelectric tunnel junction and spin-Hall-assisted spin-transfer torque
Y. Gang	5th November 2015	Université de Grenoble Alpes / Prof. L. Anghel	Reviewer	Conception d'un micro-réseau intégré NOC tolérant les fautes multiples statiques et dynamiques
A. Ravelomanantsoa	9th November 2015	Université de Lorraine / Prof. H. Rabah	Reviewer	Approche déterministe de l'acquisition comprimée et la reconstruction des signaux issus de capteurs intelligents distribués
M. Vallet	23rd November 2015	Université de Bordeaux / Prof. Y. Deval	Reviewer	Synthèse de fréquence multi-bandes couvrant les ondes millimétriques pour les applications WiFi-WiGig
I. Ouerghi	4th December 2015	Université de Grenoble Alpes / Dr. T. Ernst	Reviewer	Etude physique et evaluation des performances de NEMS à nanofils polycristallins pour la détection et l'intégration hétérogène 3D ultra-dense
S. Senni	14th December 2015	Université de Montpellier / Prof. L. Torres	Chairman	Exploration d'architecture de processeur à technologie mémoire non volatile MRAM
D. Garbin	15th December 2015	Université de Grenoble Alpes / Dr. G. Ghibaudo	Chairman	Etude de la variabilité des technologies PCM et OxRAM pour leur utilization en tant que synapses dans les systèmes neuromorphiques
L. Andrade	12th January 2016	Université Paris 6 / Prof. F. Pecheux	Reviewer	Principes et réalisation d'une interface de synchronization interopérable entre modèles de calcul SystemC AMS pour le prototypage virtuel optimisé de systèmes multi-disciplines
F. Li	29th March	Université de Nice	Reviewer	Simulation multi-moteurs multi-niveaux pour la validation des

	2016	Sophia Antipolis / Prof. G. Jacquemod		spécifications système et optimization de la consummation
M. Garci	May 2016	Université de Strasbourg / Prof. L. Hébrard	Reviewer	Simulation multi-physiques de circuits intégrés pour la fiabilité
M. Andraud	14th June 2016	Université de Grenoble Alpes / Dr. E. Simeu	Chairman	Solutions pour l'auto-adaptation des systèmes de communication sans fil
F. Berthier	8th December 2016	INRIA / Prof. O. Sentieys	Chairman	Etude et conception d'un coeur de processeur asynchrone ultra basse consommation pour les noeuds de capteurs communicants
C. Jacquemod	14th December 2016	Université Aix-Marseille / Prof. K. Aguir	Reviewer	Microcapteurs de courant non-intrusifs autonomes sur support souple
A. Vincent	3rd February 2017	Université Paris-Saclay / Dr. D. Querlioz	Reviewer	Vers une utilization synaptique de composants mémoires innovants pour l'électronique neuro-inspirée
E. Deng	10th February 2017	Université Grenoble Alpes / Prof. L. Anghel	Reviewer	Conception et développement de circuits logiques de faible consommation et fiables basés sur des jonctions tunnel magnétiques à écriture par transfert de spin
Y. Wang	13th February 2017	Télécom ParisTech / Prof. L. Naviner	Reviewer	Analyse de Fiabilité de Circuits Logiques et de Mémoire basés sur Dispositif Spintronique
C. Ben Aoun	12th July 2017	Université Pierre et Marie Curie / Prof. F. Pecheux	Chairman	Design of a virtual prototyping framework for composable heterogeneous systems
Q. An	5th October 2017	Université Paris-Saclay / Prof. J.O. Klein	Examiner	Compact modeling and circuit design based on spin injection
A. Charif	17th November 2017	Université Grenoble Alpes / Prof. M. Nicolaidis	Reviewer	Design, Parallel Simulation and Implementation of High-Performance Fault-Tolerant Network-on-Chip Architectures
G. Gourlat	29th November 2017	Université Grenoble Alpes / Dr. G. Sicard	Reviewer	Conception de circuit intégré pour les applications gravimétriques basées sur l'utilization de résonateurs mécaniques arrangés en réseau
A. Levisse	6th December 2017	Université Aix-Marseille / Prof. J.M. Portal	Chairman	Architecture, Design and Technology Guidelines for Crosspoint Memories
A. Brière	8th December 2017	Université Pierre et Marie Curie / Prof. F. Pecheux	Examiner	RF Network on Chip
D. Vodenicarevic	15th December 2017	Université Paris-Saclay / Dr. D. Querlioz	Reviewer	Utilisation de nanocomposants oscillateurs pour le calcul
E. Rosati	5th April 2018	Université de Strasbourg / Prof. C. Lallement	Reviewer	Design tools for biological systems engineering
A. Sivasan	29th June 2018	Université Grenoble Alpes / Prof. L. Anghel	Chairman	Conception et Simulation des Circuits Numériques en 28nm FDSOI pour la Haute Fiabilité
S. Hedayat	18th September 2018	Université de Lille / Prof. A. Cappy, Prof V. Hoel	Examiner	Design and fabrication of artificial neurons for bio-inspired computing
M. Julien	23rd November 2018	Université de Montpellier / Prof. G. Cathébras	Chairman	Solutions to improve the performance of dynamic CMOS current mirrors: Application to the design of current sources for biomedical devices
G. Takam	12th December 2018	Université Grenoble Alpes / Dr. E. Simeu	Chairman	Performance monitoring and error reconciliation in image decoders
P. Talatchian	9th January 2019	Université Paris-Saclay / Dr. J. Grollier	Reviewer	Bio-inspired computing leveraging the synchronization of magnetic nano-oscillators
R. Boumchedda	20th May 2019	Université Grenoble-Alpes / Dr. E. Beigné	Reviewer	Ultra-low voltage and energy-efficient SRAM design with new technologies for IoT applications
J. Liang	17th June 2019	Université de Montpellier / Dr. A. Todri-Sanial	Reviewer	Investigation of carbon nanotubes for local interconnects
M.A. Zidane	16th December	Université de	Examiner	Dispositif integré pour la mesure non invasive de la glycémie

	2019	Lorraine / Prof. A. Rouane		
K. Alhaj Ali	13th July 2020	Université Bretagne Loire / Prof. J.P. Diguet	Reviewer	New design approaches for flexible architectures and in-memory computing based on memristor technologies
T. Vayssade	15th October 2020	Université de Montpellier / Prof. L. Latorre	Reviewer	Une approche digitale pour le test faible coût de circuits intégrés RF : Application à un transceiver Zigbee
F. Ouattara	6th November 2020	Université de Montpellier / Prof. L. Torres	Examiner	Primitives de sécurité à base de mémoires magnétiques
T. Hirtzlin	18th November 2020	Université Paris-Saclay / Dr. D. Querlioz	Reviewer	Digital Implementation of Neuromorphic systems using Emerging Memory devices
R. Gauchi	22nd March 2021	Université Grenoble Alpes / Dr. P. Vivet	Reviewer	Exploration of reconfigurable tiles of computing-in-memory architecture for data-intensive applications
A.R. Ismail	28th January 2022	Université de Lorraine / Prof. H. Rabah	Chairman, Reviewer	Commensurable and Chaotic NCVO Study for Information Processing
W. Simon	26th April 2022	EPFL, CH / Prof. D. Atienza	External Reviewer	In-Memory Hardware and Architectural Extensions for Workloads Acceleration
S. Engels	1st July 2022	Grenoble INP / Dr. L. Fesquet	Chairman	Design for energy efficiency in integrated circuits
E. Quisbert	26th September 2022	U. Grenoble Alpes / Dr. T. Ernst	Member	Design methodology for sustainable IOT device
M. Ezzadeen	12th December 2022	Aix-Marseille Université / Prof. J.M. Portal	Reviewer	Circuit design for in-memory computing with innovative 3D technologies
K. Hérissé	16th December 2022	Université de Lille / Dr. A. Kaiser, Dr. A. Frappé	Chairman, Reviewer	Mixed-Signal In-Memory Matrix-Vector Multiplication for Ultra-Low Power Embedded Machine Learning
F. Jebali	6th July 2023	Aix-Marseille Université / Prof. J.M. Portal	Chairman	Design of mixed system (RRAM memory & digital) targeting binary neural network hardware accelerator
S. Bhat	11th July 2023	U. Massachussetts Amherst, USA / Prof. A. Moritz	External reviewer	Skybridge 2.0: A fine-grained vertical 3D-IC technology for future ICs
M. Rios	25th July 2023	EPFL, CH / Prof. D. Atienza	External reviewer	EdgeAI-Aware Design of In-Memory Computing Architectures
C. Delacour	19th December 2023	U. Montpellier / Prof. A. Todri-Sanial	Reviewer	Architecture Design for Analog Oscillatory Neural Networks
T.M. Shahroodi	12th March 2024	TU Delft / Prof. S. Hamdioui	External reviewer	Computation-In-Memory for Modern Applications Using Emerging Technologies
M. Martemucci	9th December 2024	U. Bordeaux / Prof. S. Saighi	Reviewer	Exploration de techniques d'apprentissage pour l'edge AI exploitant des mémoires non-volatiles
M. Toubeix	10th March 2025	U. Grenoble Alpes / Prof. T. Meunier	Examiner	Architecture and design of an ambient-temperature feedback loop between the measurement and control chains of cryogenic-temperature semiconductor qubits
L. Zulberti	17th April 2025	U. Pisa / Prof. L. Fanucci	External reviewer	CGR-AI Engine: Design and characterization of Coarse-Grained Reconfigurable Array Architectures for Artificial Intelligence in Space Applications
A. Douadi	23rd September 2025	U. Grenoble Alpes / Dr. G. Di Natale	Examiner	Design, Characterization and Security Evaluation of Physically Unclonable Functions
M. Culot	21st January 2026	U. Grenoble Alpes / Prof. J.P. Attane	Reviewer	Memristive switching in GeTe-based ferroelectric Schottky diodes for neuromorphic computing
Z. Zheng	5th June 2026	TU Munich / Prof. U. Schlichtmann	External reviewer	Design Automation and Optimization for Wavelength-Routed Optical Networks-on-Chip Across Crossbar, Ring, and Distributed Structures
M. Alsukour	9th November 2026	U. Grenoble Alpes / Prof. E. Pistono	Examiner	3D microelectronic integration for millimeter-wave applications

N. Kavand	10th November 2026	TU Dresden / Prof. A. Kumar	External reviewer	Secure circuit design using reconfigurable field effect transistors
J. Cornejo	3rd December 2026	U. Lille / Prof. A. Frappé	Reviewer	Low-Power Transformer Accelerators for Efficient Edge AI in 18nm FD-SOI CMOS
C. Ciocan	10th December 2026	CEA Saclay / M. Thévenin	Chairman	Architecture des microprocesseurs pour le traitement du signal en flot de données
A. Romdhane	14th December 2026	CEA Grenoble / G. Prenat	Chairman	AdAptive microcontroller platform for edge AI systems

Professorial dissertations

Name	*Date*	*University*	*Role*	*Title of thesis*
C. Seassal	9th March 2007	Ecole Centrale de Lyon	Examiner	Micro-Nanophotonique active III-V/silicium à base de cristaux photoniques et de microdisques
X. Letartre	3rd June 2008	Ecole Centrale de Lyon	Examiner	Micro et nano structures de semiconducteurs pour la micro-opto-électronique
J.O. Klein	30th April 2009	Université Paris Sud 11	Reviewer	Impact des technologies sur les architectures de calcul
P. Maurine	10th December 2009	Université Montpellier 2	Reviewer	Contribution à la modélisation et à la robustesse des circuits intégrés CMOS en technologie nanométrique
N. Lewis	9th April 2010	Université Bordeaux 1	Reviewer	Méthodes de conception des circuits intégrés analogiques et mixtes – Perspectives sur les systèmes électroniques en interaction avec le vivant
P.Desgreys	30th September 2010	Université Paris 6	Reviewer	Interface analogique numérique pour les télécommunications: modélisations et conceptions flexibles
F. Clermidy	7th April 2011	Université de Grenoble	Chairman	Contribution à l'évolution des architectures numériques: Des réseaux sur puce aux structures moléculaires
F. Pecheux	5th December 2011	Université Paris 6	Reviewer	Modèles de calcul interopérables et optimisés pour la modélisation multi-niveaux et la simulation efficace de systèmes homogènes et hétérogènes complexes
V. Derycke	3rd February 2012	Université Paris Sud 11	Reviewer	Transistors à nanotubes de carbone pour l'électronique haute fréquence et les circuits à apprentissage
D. Galayko	7th December 2012	Université Paris 6	Reviewer	Perspectives des systèmes intégrés sur puce: énergie et synchronisation
F. Mieyeville	29th May 2013	Ecole Centrale de Lyon	Examiner	Méthodes de conception hiérarchique de systèmes hétérogènes multi-physiques communicants
M.M. Louerat	3rd July 2013	Université Paris 6	Reviewer	Circuits analogiques documentés et réutilisables: synthèse analogique sous l'œil du concepteur
D. Navarro	23rd October 2013	Ecole Centrale de Lyon	Examiner	Modélisation et simulation de systèmes de capteurs hétérogènes
J.B. Kammerer	2nd December 2013	Université de Strasbourg	Examiner	Outils et Méthodes pour la Conception de Systèmes Intégrés Hétérogènes – Application à l'Instrumentation
A. Todri-Sanial	31st March 2015	University of Montpellier	Reviewer	Design space exploration of emerging technologies for energy efficiency
V. Fresse	3rd November 2015	Université Jean Monnet Saint-Etienne	Chairman	Conception d'architectures embarquées multi-coeurs dédiées aux applications de traitement d'images
P. Benoit	16th November 2015	Université de Montpellier	Reviewer	Systèmes numériques adaptatifs
D. Querlioz	5th April 2016	Université Paris Sud	Reviewer	La nanoélectronique : nouvelles physiques, nouvelles architectures
S. Le Beux	17th March 2017	Ecole Centrale de Lyon	Examiner	Design Methods for Emerging Technologies Based Computing Systems
M. Bocquet	23rd June 2017	Université Aix-Marseille	Reviewer	Caractérisation et modélisation compacte de mémoires émergentes
M. Madec	27th June 2019	Université de Strasbourg	Reviewer	Environnement CAO pour les systèmes hétérogènes
P. Maris Ferreira	6th November 2019	Université Paris Sud	Reviewer	Conception optimale et instrumentation intégrée pour les environnements sévères

M. Tabaa	25th September 2020	Université de Lorraine	Examiner	Contribution à la conception des systèmes électroniques intelligents pour l'industrie du futur
G. Prenat	26th March 2021	Université Grenoble Alpes	Reviewer	Design of hybrid CMOS/Magnetic logic circuits
S. Jovanovic	24th March 2022	Université de Lorraine	Chairman	Vers les architectures et systèmes de calcul guidés par l'énergie
M. Rizk	18th October 2022	IMT Atlantique	Reviewer	Efficient architectures for high-performance embedded computing
E.I. Vatajelu	24th January 2023	Université Grenoble Alpes	Member	Emerging Memories for Dependable Computing
E. Vianello	1st February 2024	Université Grenoble Alpes	Reviewer	Resistive Memory-Based Concepts for Neuromorphic Computing
S. Cueff	18th October 2024	Ecole Centrale Lyon	Examiner	Composants nanophotoniques reconfigurables à base de matériaux à changement de phase
B. Larras	16th December 2026	U. Lille	Reviewer	In-memory and event-driven computing for ultra-low-power integrated circuits in artificial intelligence applications at the edge

Participation in faculty recruitment boards (external to ECL)

Position	*Date*	*University*	*Title of position*
Full Professor	11th May 2010	PHELMA / Grenoble INP	Design and test of digital integrated circuits
Associate Professor	25th April 2012	Université de Lorraine	Digital circuit architectures for reconfigurable computing or for sensors
Associate Professor	6th May 2013	Université Montpellier 2	Sensors, thin film deposition, instrumentation, RFID, cleanroom technology, materials, flexible substrates
Associate Professor	16th May 2013	PHELMA / Grenoble INP	Design of digital integrated circuits
Full Professor	6th May 2015	INSA Lyon	Physics / Nanotechnology
Full Professor	10th May 2016	University of Lille	Information Processing
Full Professor	11th May 2018	IUT Haguenau	Electrical Engineering
Full Professor	10th May 2019	IUT Marseille	Digital science and technology
Associate Professor	8th June 2020	PHELMA / Grenoble INP	Computer Science
Associate Professor	2nd-3rd Sept. 2021	University of Cyprus	Microelectronic Circuit Design

Principal responsibilities in scientific programs

Regional projects (Rhône-Alpes)

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
Osmose	2003–2006	ECL	Coordinator Leader for WP4 (Synthesis and design methods)	210K€ / 133K€	Outils pour la co-simulation, synthèse et modélisation de systèmes sur puce (*Tools for co-simulation, synthesis and modeling of systems on chip*)
EmSoC-Recherche	2004–2007	INP Grenoble	Leader for WP6 (Hardware architectures and heterogeneous design)	200K€ / 15K€	Systèmes embarqués (*Embedded systems*)
SEMBA	2008–2011	INP Grenoble	Leader for WP3 (Communication infrastructures for smart objects)	200K€ / 15K€	Systèmes embarqués (*Embedded systems*)
MESYCH-3D	2012–2015	ECL	Coordinator	110K€ / 100K€	Méthodes de synthèse pour circuits hétérogènes 3D (*Synthesis methods for 3D heterogeneous circuits*)
Grilles-CMOS	2012–2013	ECL	Coordinator	40K€	Evaluation système d'une cellule logique reconfigurable à base de transistors MOSFET double grille (*System-level evaluation of a double-gate MOSFET based reconfigurable logic cell*)
Auto-BAW	2016–2019	ECL	INL coordinator	110K€	Automatic Control for BAW filter Design and Analysis

National projects (France)

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
Heteropt / RMNT	2001–2004	INL-ECL	Leader for WP5 (Circuit design)	450K€ / 50K€	New technologies for heterogeneous integration of high-density optical links on silicon integrate circuits
Nanosys / ACI Nanosciences	2004–2006	IEF	Leader for WP2 (Elementary nanodevice-based functions)	300K€ / 25K€	Architectures for the integration of molecular nanodevices
Multigrilles / ANR^{PNANO}	2005–2007	CEA-LETI	Leader for WP3 (Design of novel digital and analog cells)	800K€ / 100K€	Disruptive design of elementary cells for multiple gate sub 32nm CMOS circuits
3D-IDEAS / ANR^{PNANO}	2008–2011	INL-ECL	Coordinator Leader for WP2 (Design flow)	1.5M€ / 300K€	3D integration and design technology for imager applications and systems
Nanograin / ANR^{ARPEGE}	2008–2011	CEA-LETI	Leader for WP2 (Nanograin cells and associated functions)	500K€ / 200K€	Ultra-fine grain reconfigurable architectures based on nanodevices

NHNR / CNRS–Défi G3N	2012–2013	INL-CNRS	Coordinator	7K€	Nanoprocesseur hybride neuro-reconfigurable (*Hybrid neuro-reconfigurable nanoprocessor*)
HELICITY / ANR[Générique]	2016–2019	INL-CNRS	Coordinator Leader for WP1 (Unified tool for the design and optimization of continuous-discrete and multi-physics systems)	500K€ / 150K€	Heterogeneous Component Design Technology
LEGO / ANR[Générique]	2018–2023	IMS Bordeaux	Leader for WP1 (Logic design)	500K€ / 160K€	Logic Elements using Gate Overstacking
OpticALL^2 / ANR[Générique]	2018–2024	INL-ECL	Coordinator Leader for WP1 (manycore architecture demonstrator)	575K€ / 150K€	On-chip optical interconnect for all to all communications
Octane / ANR[Générique]	2021–2025	CEA-LETI	Leader for WP4 (System-level design, modeling and demonstration)	686K€ / 220K€	silicOn photoniCs sTochastic mAtrix multiplier with phase chaNge matErials
CHOOSE / PEPR Electronique	2022–2026	CNRS / CEA	Coordinator Leader for WP1 (DTCO methods)	1M€ / 150k€	System-Design-Technology Co-optimization – Priority research and equipment program on Electronics
PEPR IA	2022–2026	CNRS / CEA / Inria	Steering committee member		Priority research and equipment program on Artificial Intelligence
FerroFutures / PEPR Electronique	2024–2028	IMS Bordeaux	INL coordinator	3M€ / 500k€	plateForme fERROélectrique pour le calcUl embarqué critique : efficaciTé, peRformancES, adaptibilité
MultiSPIN / PEPR SPIN	2025–2029	IPCMS-CNRS	INL coordinator	680k€ / 190k€	Van der Waals Multiferroic Heterostructures for Logic-In-Memory Spintronic Devices
PEPR-Agence PHOENIX	2026–2031	CEA / ECL	Scientific co-coordinator INL coordinator for PC ChipMosaic Co-coordinator for PC TOTEM	17M€ / 1.32M€	
PEPR-Agence CAMELIA	2026–2031	CEA / Inria	Co-coordinator for PC-LEAF	35M€ / 720k€	

European projects

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
PICMOS / FP6-IST-STReP	2004–2007	IMEC (BE)	Leader for WP1 (System studies, Definition of applications)	2M€ / 100K€	Photonic Integration on CMOS
WADIMOS / FP7-ICT-STReP	2007–2010	IMEC (BE)	Joint leader for WP1	2.2M€ / 240K€	Wavelength Division Multiplexed Photonic Layer on CMOS
HELIOS / FP7-ICT-IP	2008–2012	CEA-LETI (FR)	Leader for WP7.1 (Design Libraries)	5M€ / 200K€	Photonics Electronics functional integration on CMOS

3DIM3 / Eureka-CATRENE	2008–2012	STMicroelectronics (FR)	INL coordinator, leader for T4.5 (Methods and tools for system-level design)	15M€ / 350K€	3D-TSV Integration for Multimedia and Mobile Applications
H-Inception / Eureka-CATRENE	2012–2015	STMicroelectronics (FR)	INL coordinator, leader for T2.2 (Investigation of implementation concepts), WP5 Leader	10M€ / 250K€	Heterogeneous-Inception
3εFerro / H2020-ICT	2018–2021	CEA-Saclay (FR)	INL leader for WP4 (New concepts and designs for energy-efficient embedded FE computing)	4M€ / 360K€	Energy Efficient Embedded Non-volatile Memory Logic based on Ferroelectric Hf(Zr)O_2
FVLLMONTI / H2020-FETOPEN	2021–2025	IMS Bordeaux (FR)	INL coordinator, leader for WP4 (VNWFET-based 3D neural network compute cube N^2C^2 design)	4.8M€ / 580K€	Ferroelectric Vertical Low energy Low latency low volume Modules fOr Neural network Transformers In 3D
Ferro4EdgeAI / Horizon Europe - DIGITAL-EMERGING	2024–2027	CEA-Saclay (FR)	INL coordinator, leader for WP1 (Applications, metrics, baselines, simulations)	3.9M€ / 550k€	Scalable, ferroelectric-based accelerators for energy efficient edge AI

International projects

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
DMT / PICS CNRS	2008–2010	ECL / EPM	French partner coordination	45K€ / 22K€	Design methods and tools for future heterogeneous system on chip architectures