Ian O'Connor

Distinguished Professor of Cross-Layer Design for Energy-Efficient Computing

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300+	4,326	30	40	7.3 M€	9
peer-reviewed works	citations	h-index	PhD theses supervised	partner funding secured	projects coordinated

Profile

Ian O'Connor (IEEE Senior Member) is Distinguished Professor at Ecole Centrale de Lyon, joint head of the Electronics group at the Lyon Institute of Nanotechnology, Director of the CNRS GdR SoC2 research network and scientific co-director of the France 2030 PHOENIX program for advanced integrated circuit design. His research addresses energy-efficient computing beyond transistor scaling: circuits and architectures built on emerging devices, silicon photonics for on-chip and in-network computing, and design–technology co-optimization methods for heterogeneous, 3D and chiplet-based systems. He chairs the European Design Automation Association, is IEEE CEDA Vice-President for Publications, and was General Chair of DATE 2023.

Current positions and roles

2007–	**Professor, now Distinguished Professor** — Ecole Centrale de Lyon, Department of Electronic, Electrical and Control Engineering
2007–	**Joint head, Electronics group (about 25 faculty)** — Lyon Institute of Nanotechnology (INL)
2026–2031	**Scientific co-director, PHOENIX** — France 2030 national hub for advanced IC design (17 M€)
2018–	**Director, GdR SoC2** — CNRS national research network on SoC, embedded systems and IoT
2026–	**Chair, Main Board** — European Design and Automation Association (EDAA)
2026–2027	**Vice-President for Publications** — IEEE Council on Electronic Design Automation (CEDA)
2026–2027	**Area Editor, Circuits and Emerging Technologies** — IEEE Trans. Computer-Aided Design (TCAD)
2024–	**Associate Editor** — IEEE Trans. Circuits and Systems for Artificial Intelligence
2023–	**Expert** — Collège Numérique France 2030; also IRDS Systems and Architectures focus team, IFIP WG 10.5

Career and education

2008–2022	**Adjunct Professor** — Ecole Polytechnique de Montréal, Canada
1998–2007	**Associate Professor** — Ecole Centrale de Lyon
1997–1998	**Senior CAD Engineer** — Philips (now NXP) Semiconductors, Southampton, UK
2005	**Habilitation (HDR)** — Ecole Centrale de Lyon
1997	**PhD in Electronics, with distinction** — University of Lille
1990–1992	**BEng and MSc (European program)** — University of Essex, ESIEE Paris, Universität Karlsruhe

Research

Emerging devices for energy-efficient edge computing. Logic, memory and in-memory computing on vertical nanowire FETs, HfO_2 ferroelectric devices (FeFET, FeMFET), reconfigurable FETs and 2D materials, from cell design to system-level evaluation.

Silicon photonics for computing. Optical networks-on-chip, thermal-aware laser control, photonic matrix multiplication with phase-change materials and stochastic computing, and photonic neural networks on lithium niobate.

Design–technology co-optimization. Predictive multi-physics synthesis (patented), 3D IC floorplanning, analog variability estimation, and DTCO/STCO methodologies for chiplet-based and near-memory architectures.

Major projects

Project	Program	Period	Funding total / partner	Role
PHOENIX	France 2030 PEPR-Agence	2026–2031	17 M€ / 1.32 M€	Scientific co-coordinator
CAMELIA (LEAF)	France 2030 PEPR-Agence	2026–2031	35 M€ / 720 k€	Co-coordinator, LEAF
Ferro4EdgeAI	Horizon Europe	2024–2027	3.9 M€ / 550 k€	INL coordinator, WP leader
FerroFutures	PEPR Électronique	2024–2028	3 M€ / 500 k€	INL coordinator
MultiSPIN	PEPR SPIN	2025–2029	680 k€ / 190 k€	INL coordinator
CHOOSE	PEPR Électronique	2022–2026	1 M€ / 150 k€	Coordinator, WP leader
FVLLMONTI	H2020 FET-Open	2021–2025	4.8 M€ / 580 k€	INL coordinator, WP leader
3D-IDEAS	ANR	2008–2011	1.5 M€ / 300 k€	Coordinator, WP leader
3DIM3, H-Inception	Eureka CATRENE	2008–2015	25 M€ / 600 k€	INL coordinator, task leader

Coordinator of 9 projects (about 4 M€ total budget) and work-package leader in 19; about 7.3 M€ in partner funding secured for INL/ECL across 30 funded projects since 2001.

Supervision

40 PhD theses (31 defended, 9 ongoing), 12 postdoctoral researchers and 28 MSc interns. Graduates hold positions at IBM Research, CERN, EPFL, University of Utah, NTU Singapore, CEA-LETI, STMicroelectronics, Cadence, Synopsys and Siemens EDA, and have founded or joined start-ups (eVaderis, Luceda). One thesis received the Best Centrale Innovation Thesis Award.

Service and recognition

- **Conferences:** General Chair DATE 2023 (Program Chair 2021, Vice-General Chair 2022), DCIS 2018, VLSI-SoC 2016 and 2026 (co-chair); Program Chair NANOARCH 2011 and 2015, ISVLSI 2008, MCSoC 2016; DAC Emerging Technologies track chair 2025–2027
- **Editorial:** IEEE TCAD (Associate Editor 2022–2025, Area Editor 2026–2027), IEEE TCASAI, IET CDT, IEEE TMSCS; guest editor for IEEE Trans. Nanotechnology, ACM JETC and others
- **Evaluation:** European Innovation Council, ERC, MSCA, Horizon Europe, ANR committees (vice-president 2015), HCERES committee chair (IEMN, 2024); external reviewer for 90 PhD theses
- **Awards:** IEEE CEDA Outstanding Service Recognition (2024); IEEE TTTC Outstanding Service Award (2023); Best Paper Awards, VLSI-SoC 2025 and IEEE NEWCAS 2011; National Scientific Excellence Award, seven consecutive awards 2001–2028

Selected publications

- I. O'Connor, J. Liu, F. Gaffiot et al., "CNTFET Modeling and Reconfigurable Logic Circuit Design," *IEEE Trans. Circuits and Systems I*, 54(11), 2007.
- I. O'Connor, F. Tissafi-Drissi, F. Gaffiot et al., "Systematic Simulation-Based Predictive Synthesis of Integrated Optical Interconnect," *IEEE Trans. VLSI Systems*, 15(8), 2007.
- H. Filiol, I. O'Connor, D. Morche, "Analog IC variability bound estimation using the Cornish-Fisher expansion," *IEEE Trans. CAD*, 31(9), 2012.
- F. Frantz, L. Labrak, I. O'Connor, "3D IC floorplanning: automating optimization settings and exploring new thermal-aware management techniques," *Microelectronics Journal*, 43(6), 2012.

- H. Li, A. Fourmigue, S. Le Beux, I. O'Connor, G. Nicolescu, "Towards maximum energy efficiency in nanophotonic interconnects with thermal-aware on-chip laser tuning," *IEEE Trans. Emerging Topics in Computing*, 6(3), 2018.
- A. Perodou, A. Korniienko, G. Scorletti et al., I. O'Connor, "Frequency Design of Lossless Passive Electronic Filters," *IEEE Trans. Circuits and Systems I*, 68(1), 2021.
- C. Marchand, I. O'Connor, M. Cantan, S. Slesazeck, T. Mikolajick, "A FeFET-based hybrid memory accessible by content and by address," *IEEE JXCDC*, 8(1), 2022.
- M. Abdalla, C. Zrounba, R. Cardoso et al., I. O'Connor, F. Pavanello, "Minimum complexity integrated photonic architecture for delay-based reservoir computing," *Optics Express*, 31(7), 2023.
- R. Cardoso, C. Zrounba, M. Abdalla et al., I. O'Connor, S. Le Beux, "Reconfigurable Photonic GEMM Based on Phase-Change-Materials and Stochastic Computing," *IEEE/Optica J. Lightwave Technology*, 2024.
- M. Soliman, C. Marchand et al., I. O'Connor, A. Ouerghi, J.F. Dayen, "Van der Waals Inverted-Floating-Gate Transistors for Artificial Intelligence Electronics," *ACS Nano*, 19(19), 2025.

Complete list (66 journal articles, 4 books, 22 chapters, 235 conference papers, 7 patents) in the full CV and at ioconnor930.github.io.

Patents

- Reconfigurable logic cell based on double-gate MOSFETs — FR 07 56487, extended to EU and USA (2007)
- Reconfigurable Boolean cells based on a crossed-nanowire matrix — FR 09 58894, PCT WO2011070164 (2009)
- Crossed-topology matrix — FR 09 58957 (2009)
- Programmable static logic gate with ambipolar transistors — FR 10 59363 (2010)
- Programmable dynamic logic gate — FR 10 59364 (2010)
- Method for the optimized design of integrated electronic circuits — FR 11 61180 (2011)
- Reconfigurable interface for optical network-on-chip — FR (2014)

Recent invited talks and lectures

- **2027** Invited talk, NEUROCOM Workshop, HiPEAC 2027, Glasgow, UK (forthcoming)
- **2026** "Building Energy-Efficient, High-Performance Circuits and Architectures Tailored to Machine Learning Computation," lecture, Advanced School on AI and Intelligent Systems, Favignana, Italy
- **2025** Panel on emerging technologies and the environmental footprint of computing, GreenTech Forum, Paris
- **2025** "Next-Gen AI Hardware in Datacenters: Energy-Efficiency and other stories," ECL Alumni Ignite, London
- **2025** Position statement, panel "Navigating the tides of funding for chips and system design," DAC 2025, San Francisco
- **2025** "Next-Gen AI Hardware: Shaping the Datacenter Revolution," LID World Summit 2025, Grenoble

52 invited and keynote conference papers and 83 workshop, seminar, tutorial and panel contributions in total.

Science communication

- **The Co-Optimized Silicon Stack:** ongoing weekly series on the future of chip technology, LinkedIn, since August 2026 (14 articles to date)
- **Interviews and commentary:** EE Times (2025, on European chip policy and low-power AI chips), Semiconductor Engineering (2025, on public funding for chip design tools), Proteus Leader Show (2025, on the energy cost of AI)
- **Articles:** Scientia (2025, 3D neural networks for in-ear AI); Télécom (2022, manufacturing technologies for future systems-on-chip)

Teaching

Courses from Bachelor 3 to Master 2 at Ecole Centrale de Lyon and in international master's programs: electronic systems, digital architectures, analog computing for AI, sustainable and trustworthy hardware for AI, heterogeneous microelectronic design, nanoelectronics. Co-manager of the Electronics and Embedded Systems track of the Master EEEA; head of the Centrale Lyon electronics teaching group 2011–2019.